

FIG. 2

FIG. 3A

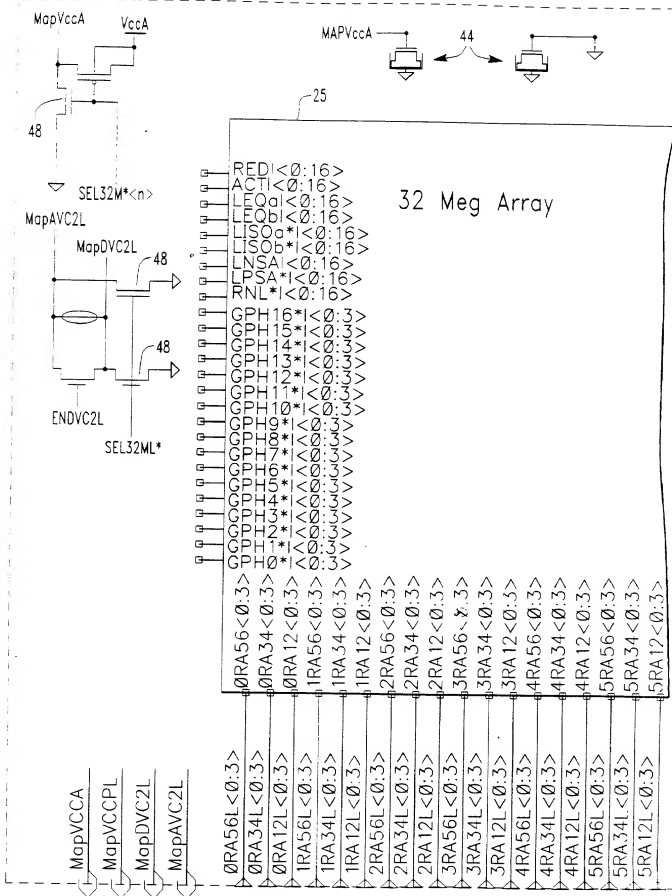


FIG. 3B

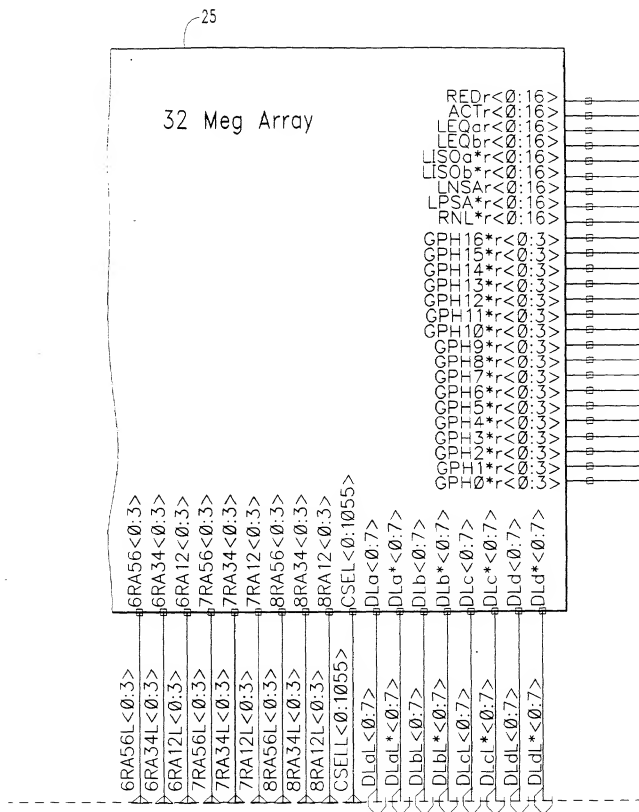


FIG. 3C

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64 Meg Array

29

glbSADriver

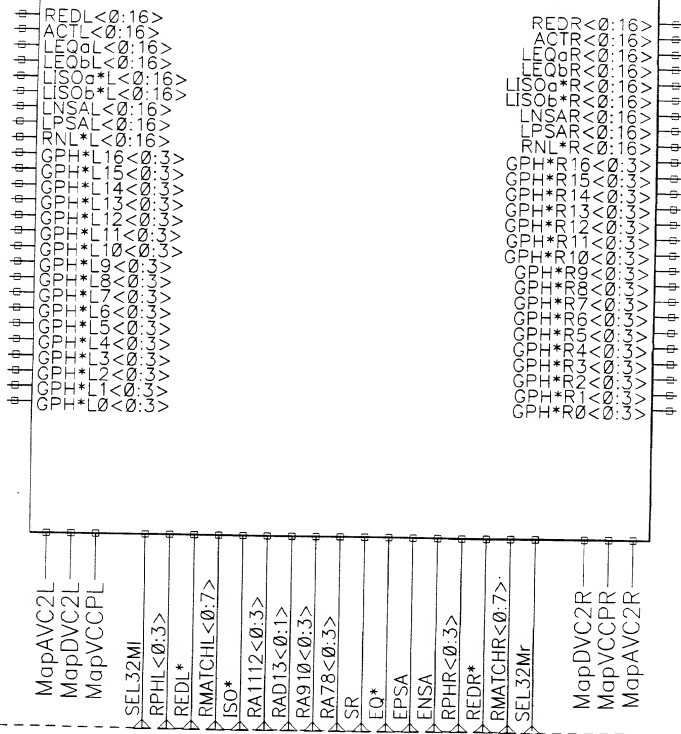


FIG. 3D

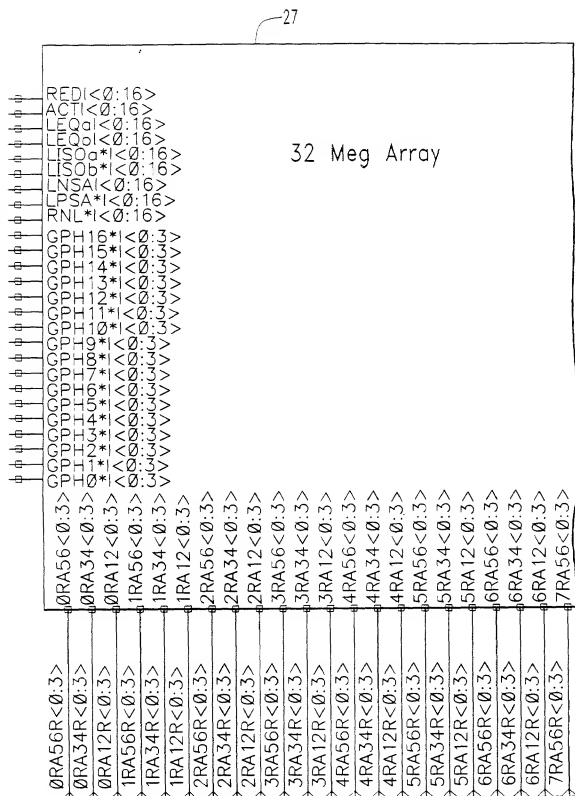
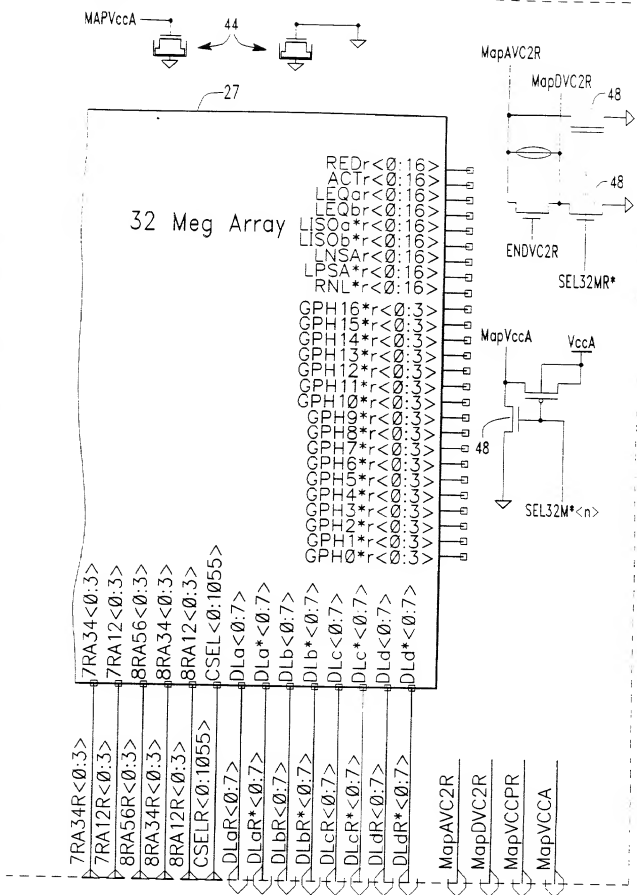


FIG. 3E



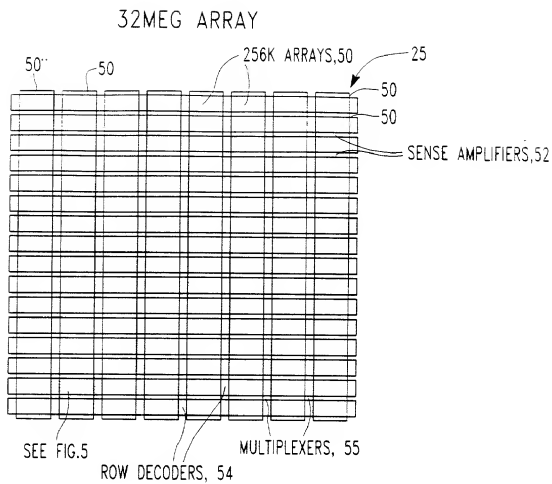


FIG. 4

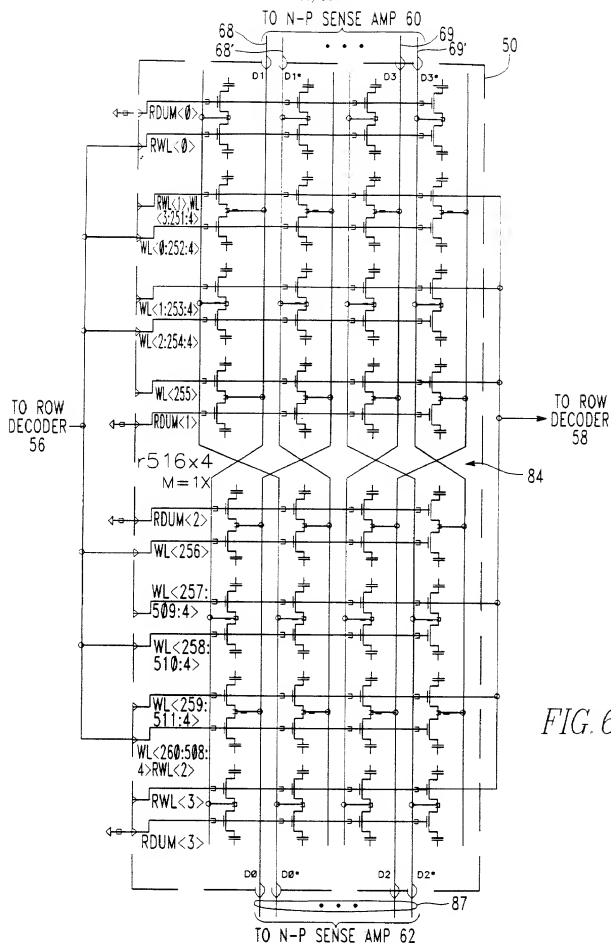
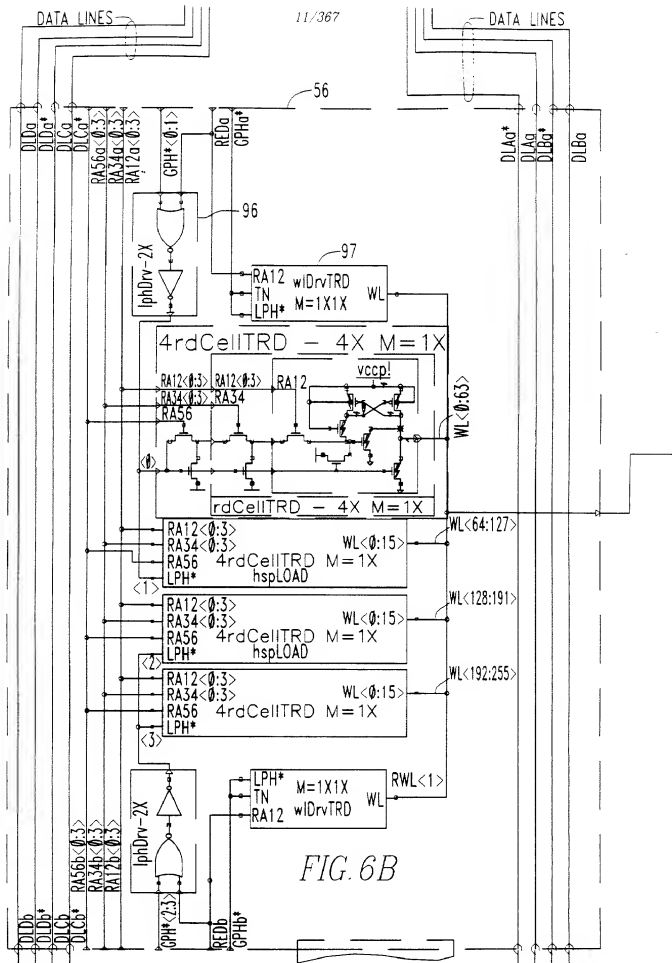
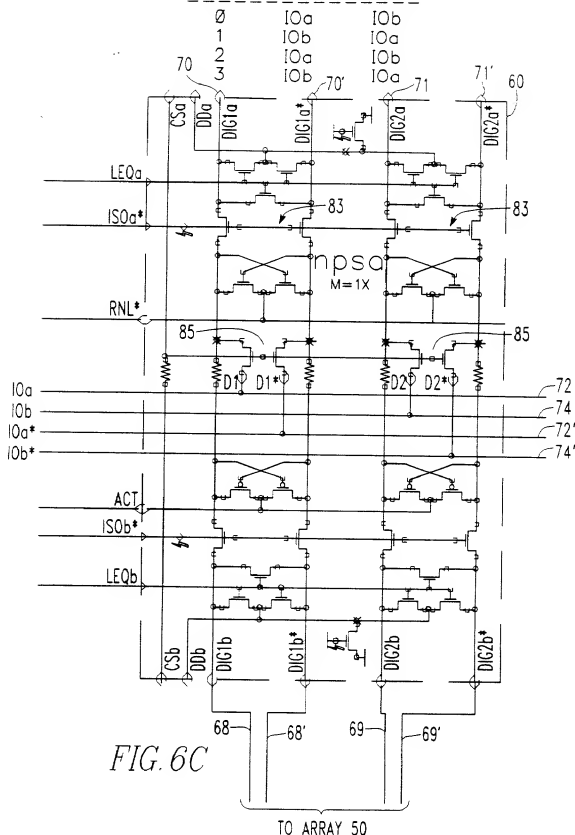


FIG. 6A



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Connections of odd/even
columns to IOa and IOb
alternates with odd/even
column select lines:
CA01* D1(even) D2(odd)



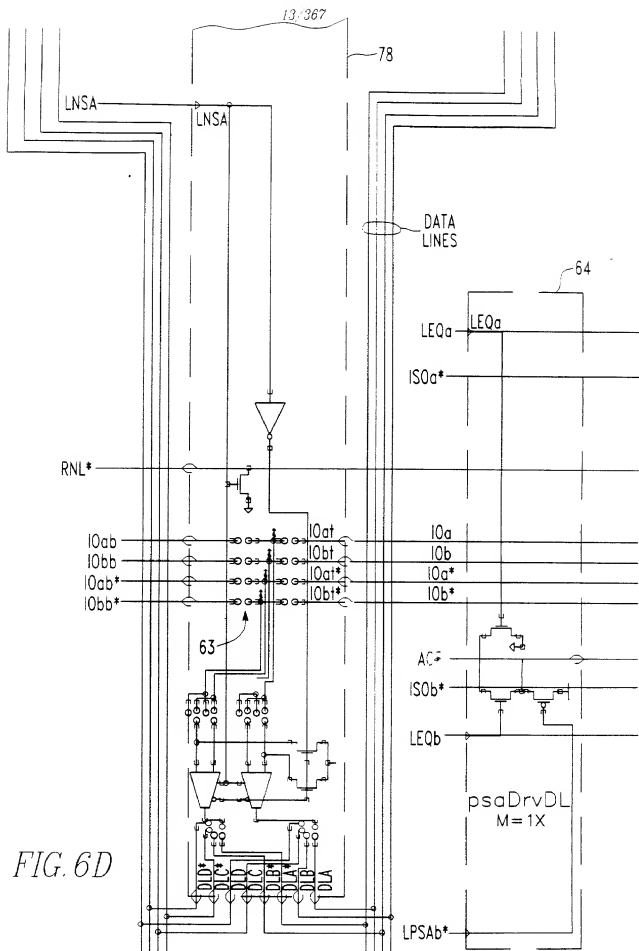


FIG. 6D



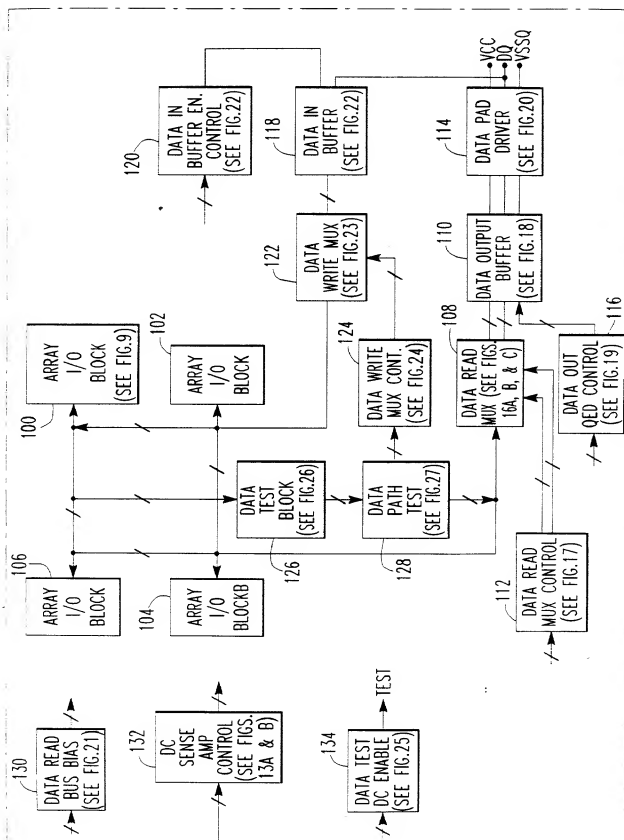


FIG. 8

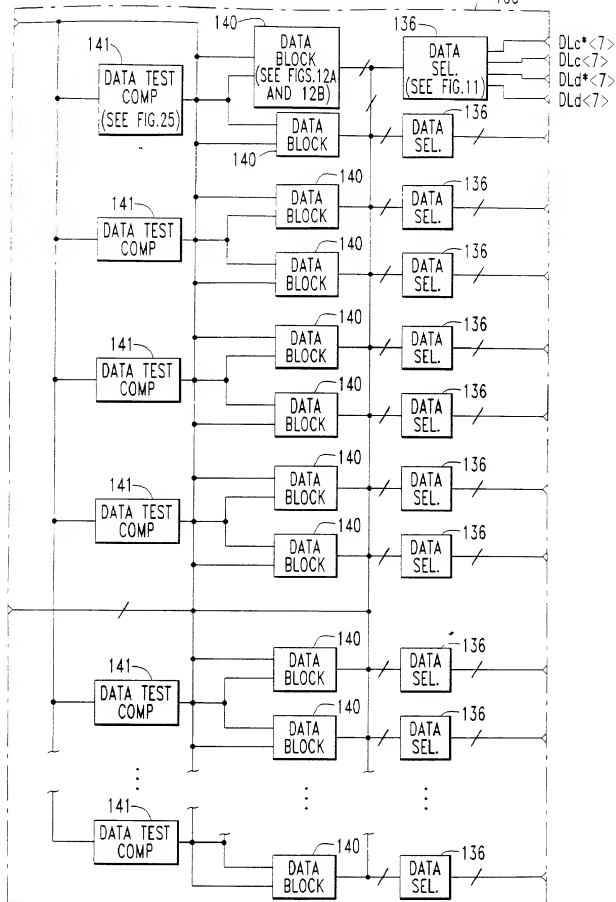
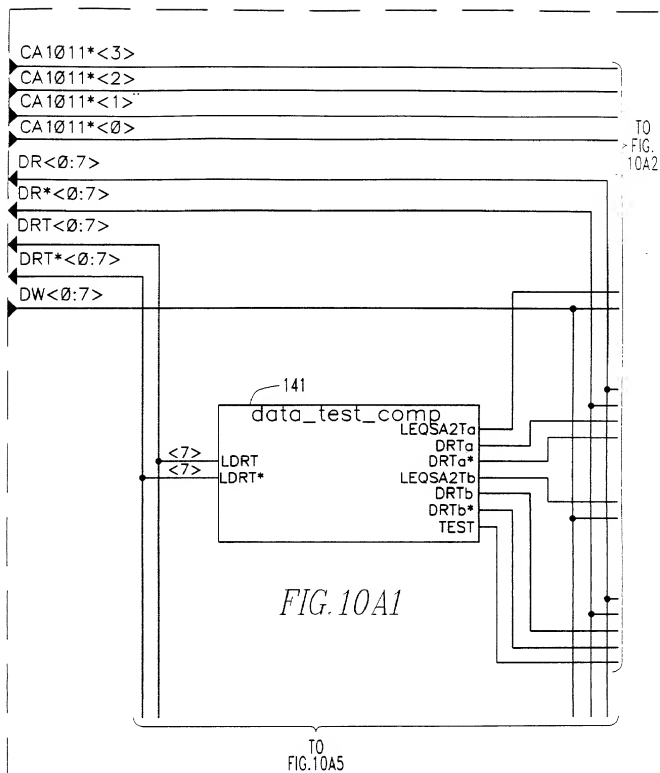


FIG. 9



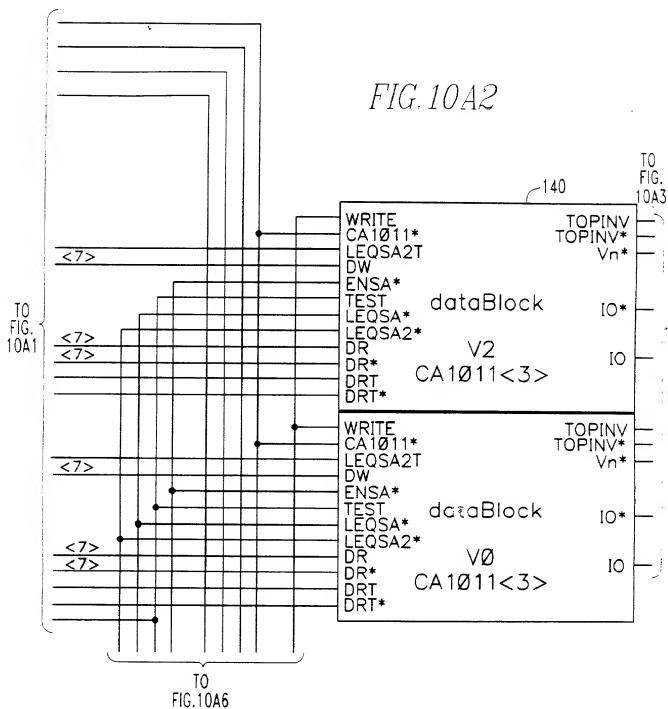
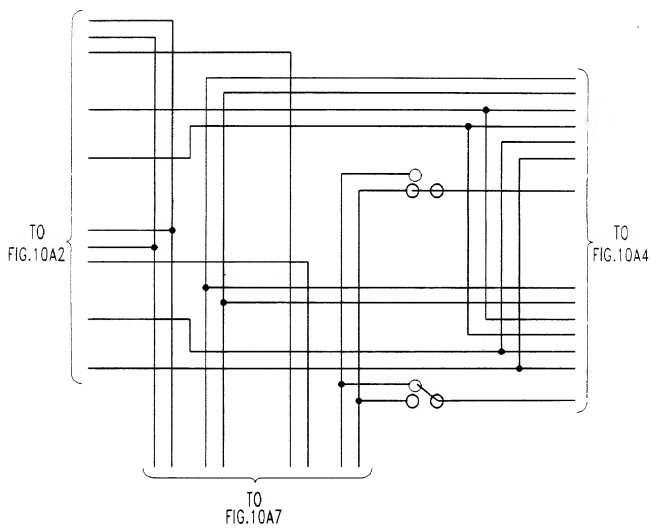


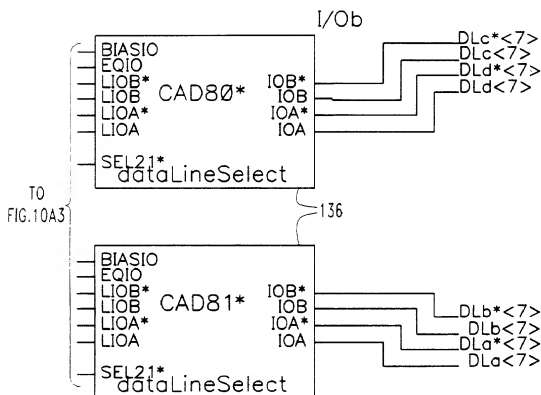
FIG. 10A3



arrayIOBlock

100

FIG. 10A4



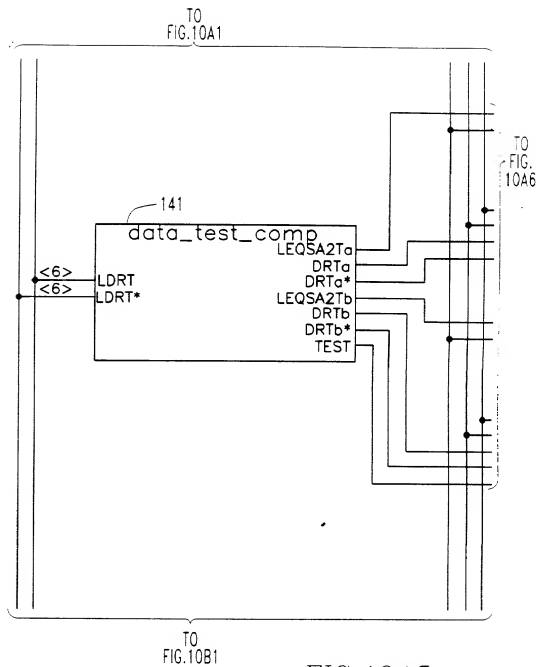


FIG. 10A5

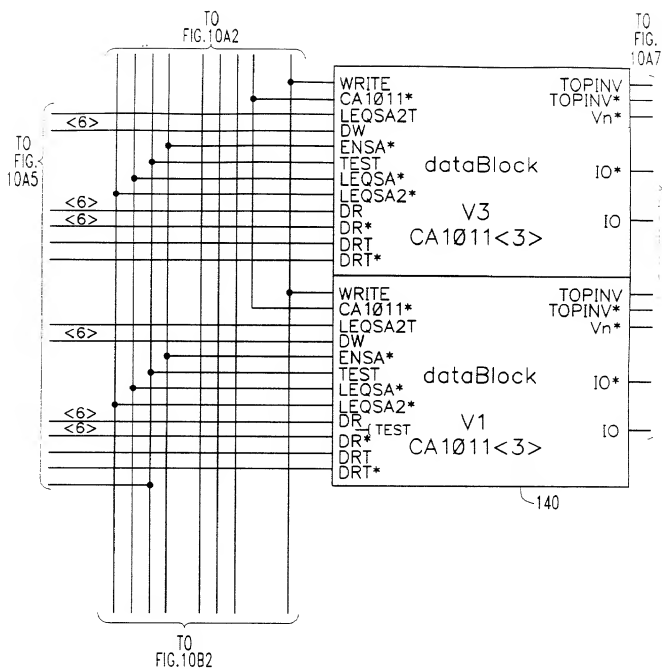


FIG. 10A6

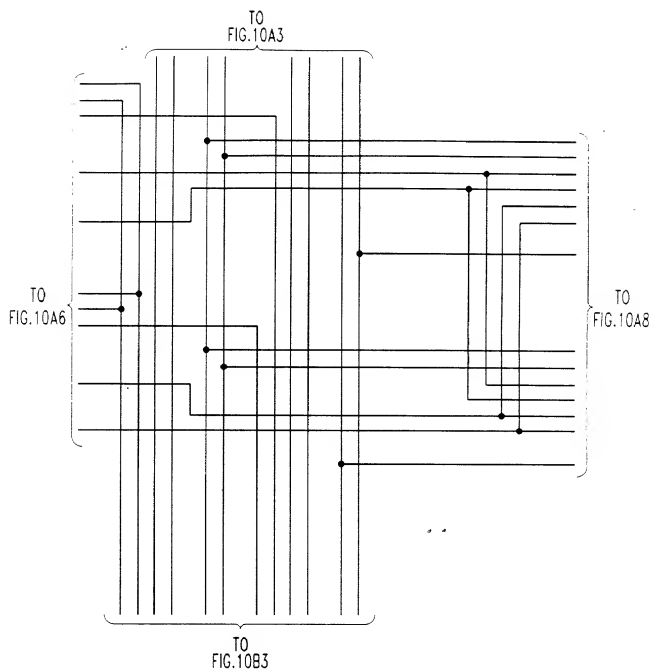


FIG.10A7

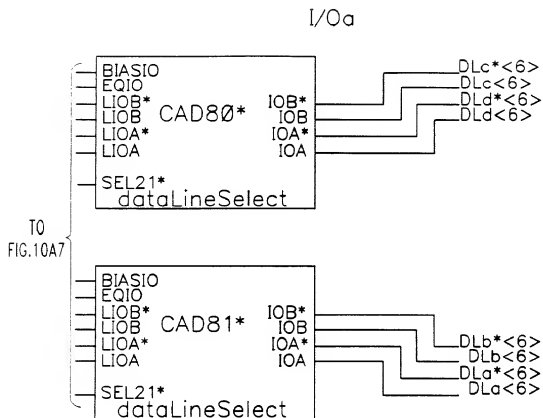


FIG. 10A8

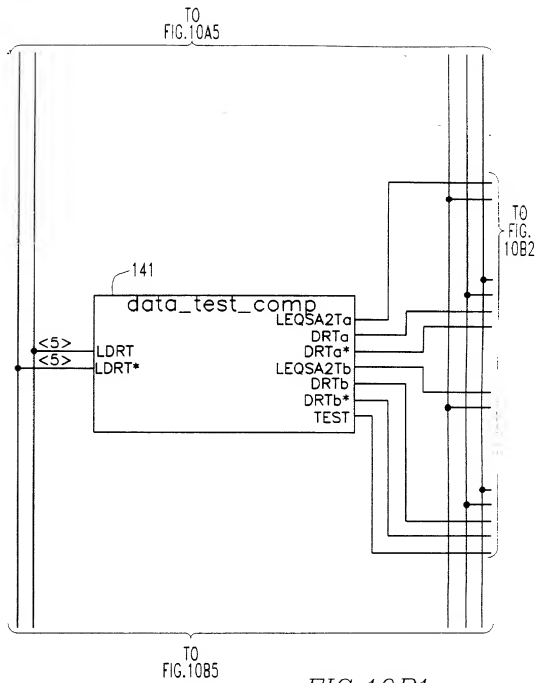


FIG. 10B1

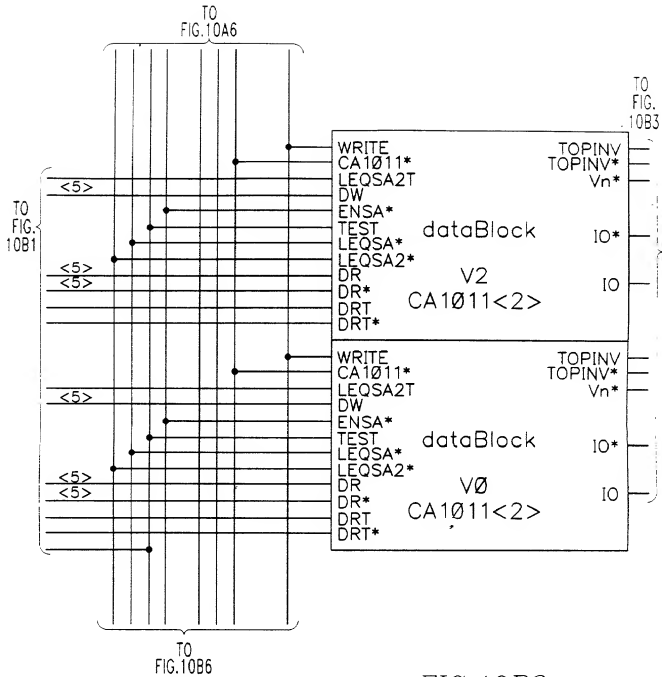


FIG. 10B2

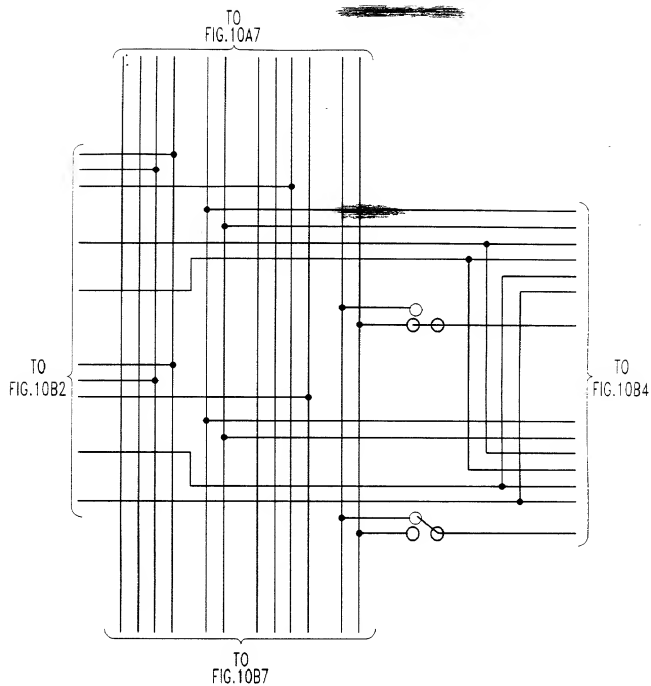


FIG. 10B3

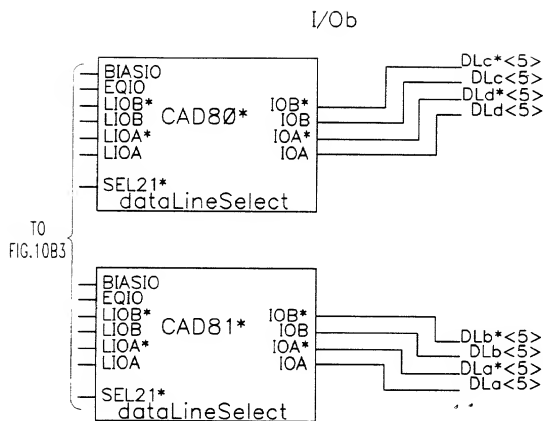


FIG. 10B4

FIG. 10B5

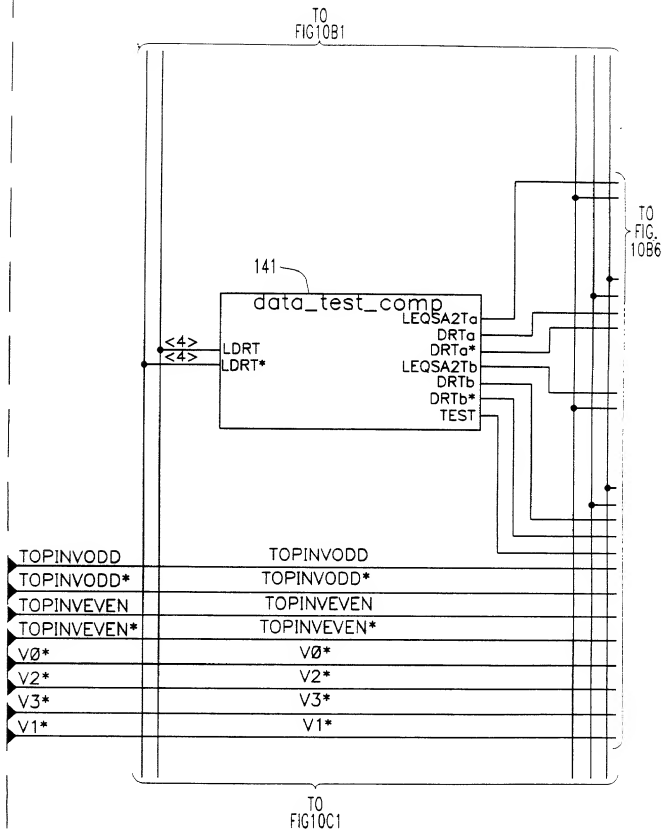


FIG. 10B6

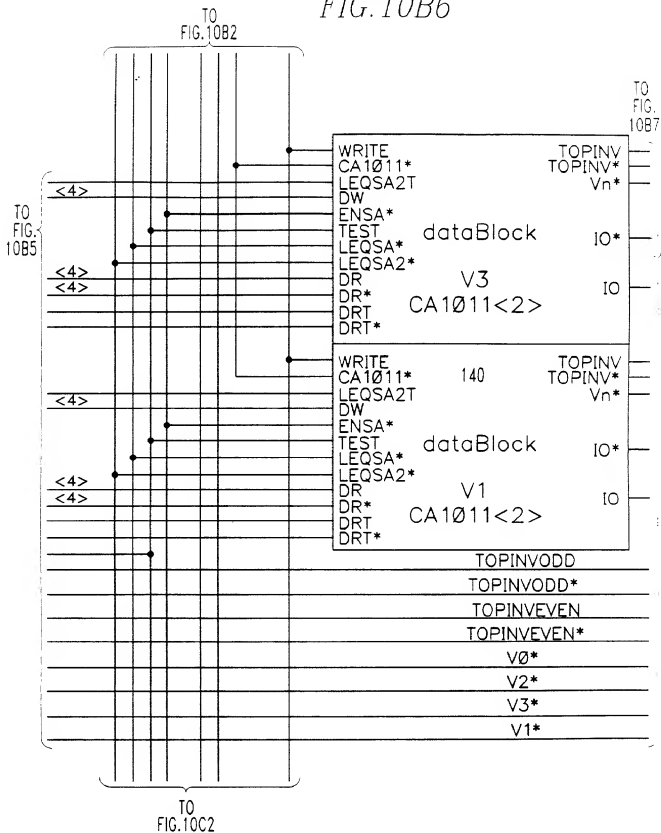
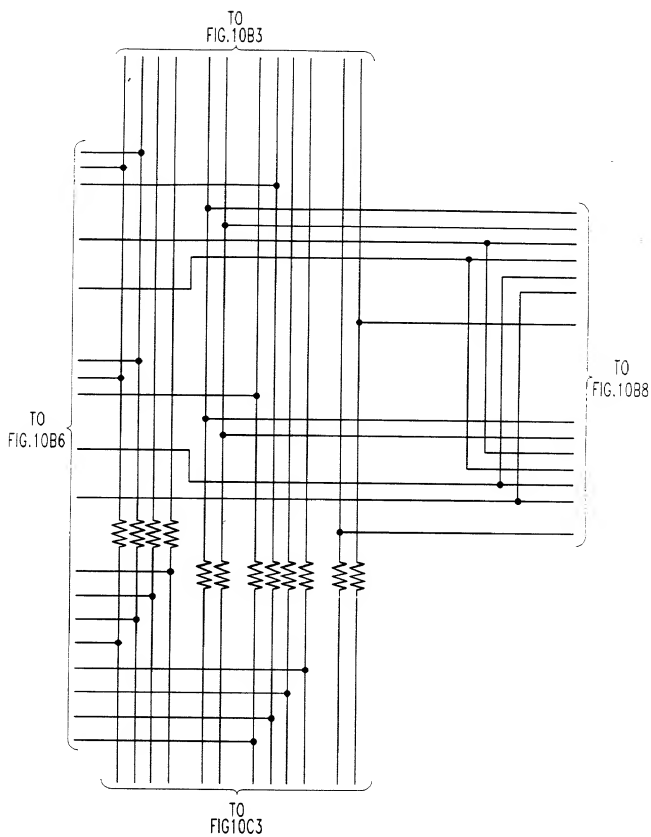
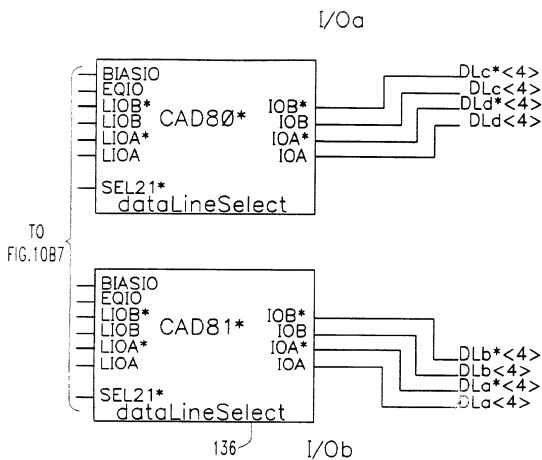


FIG. 10B7



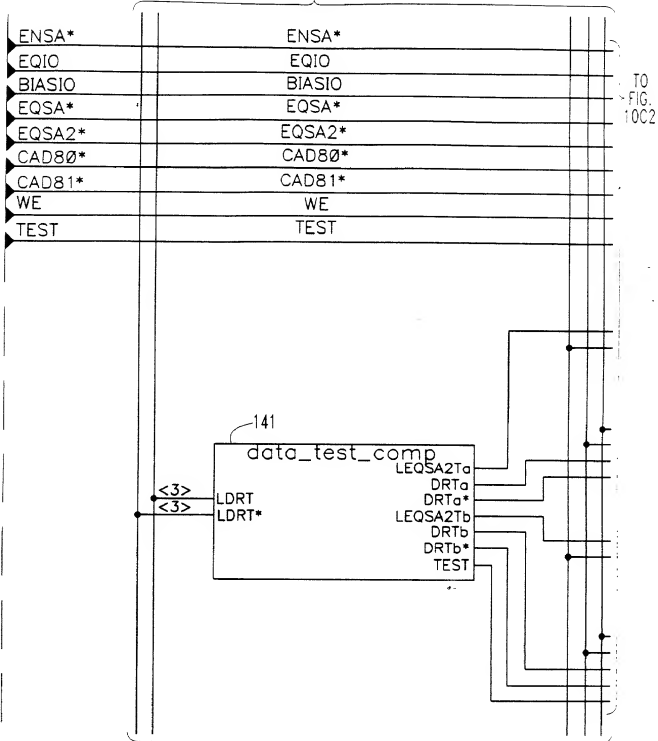
0934795.08203

FIG. 10B8



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TO
FIG. 10B5



TO
FIG. 10C5

FIG. 10C1

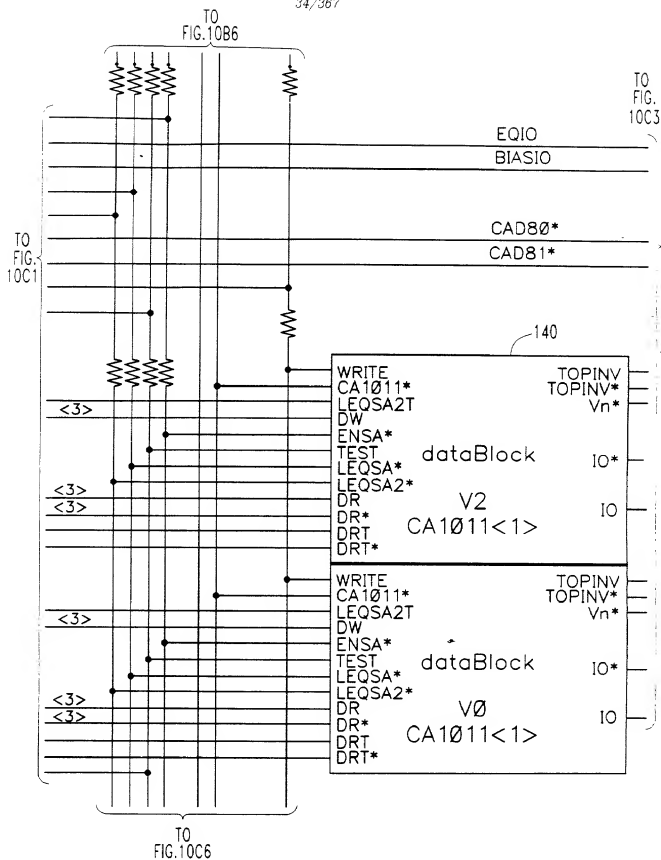
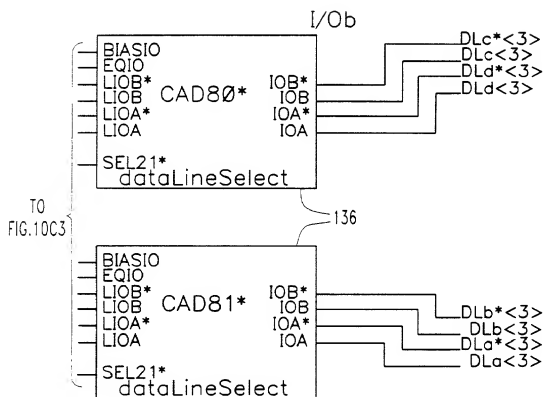


FIG. 10C2

FIG. 10C4



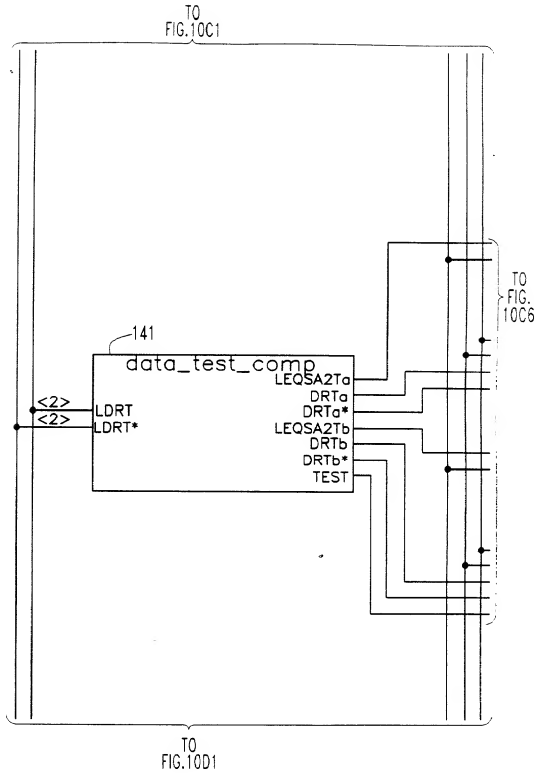


FIG. 10C5

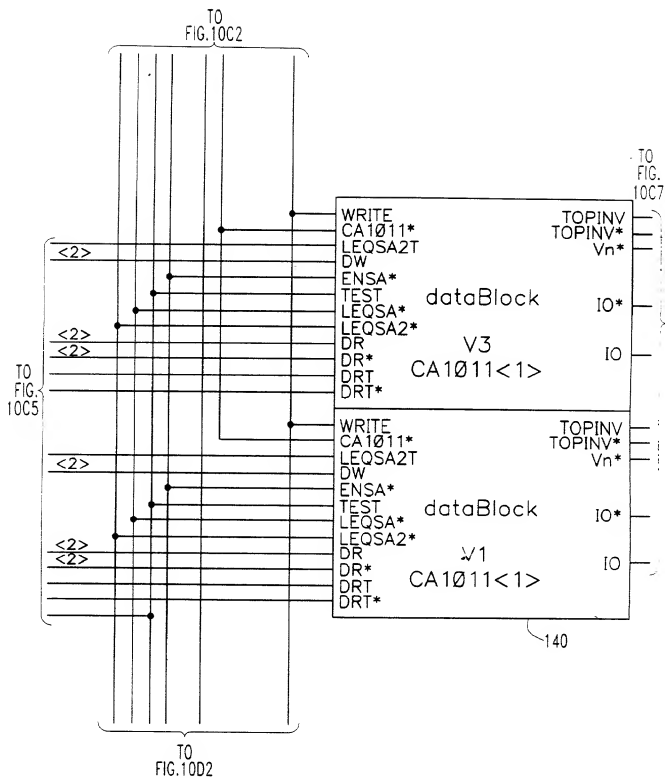


FIG. 10C6

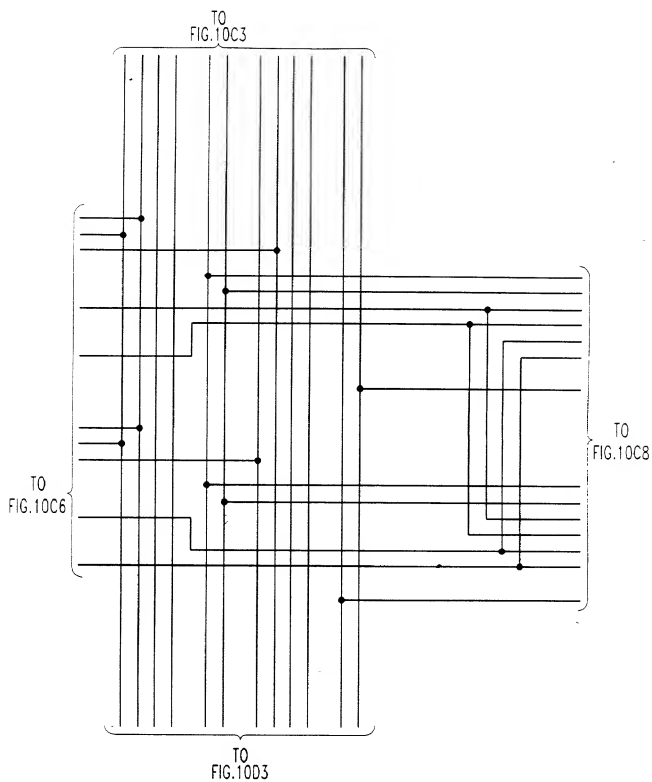


FIG.10C7

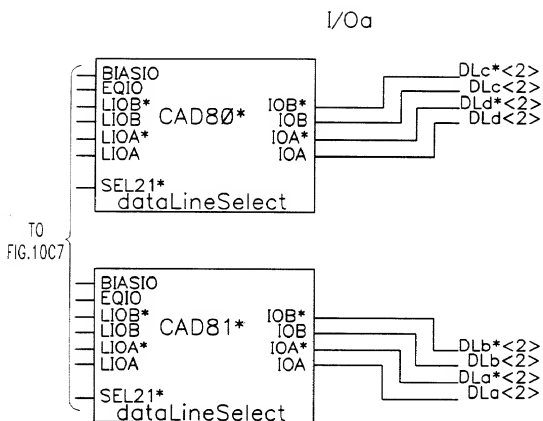


FIG.10C8

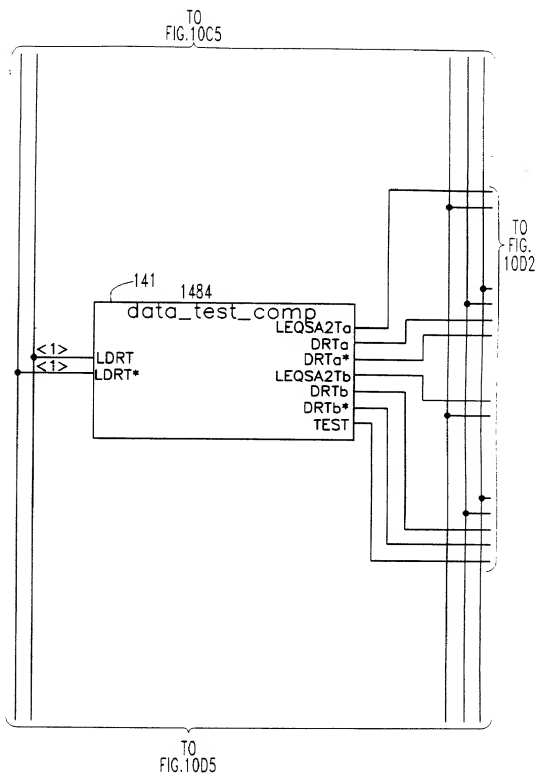


FIG. 10D1

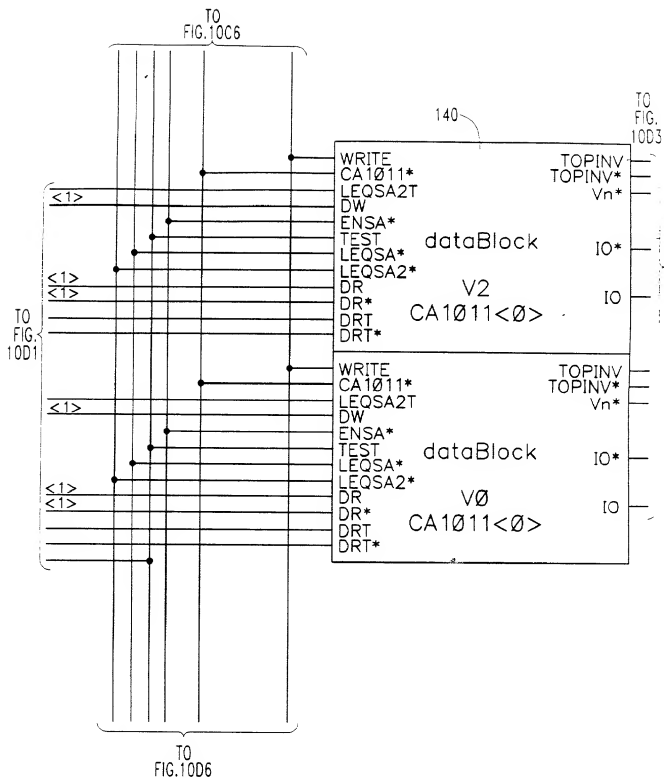


FIG. 10D2

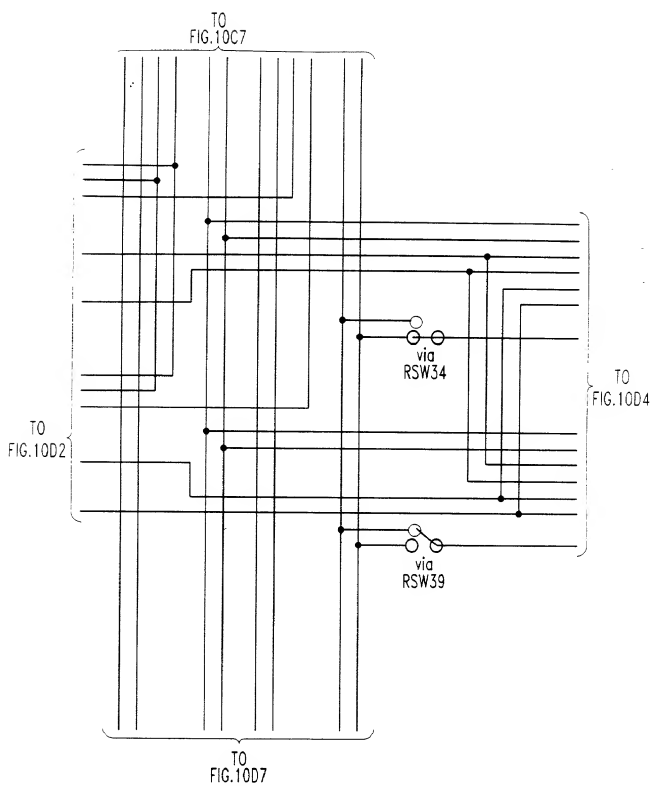


FIG. 10D3

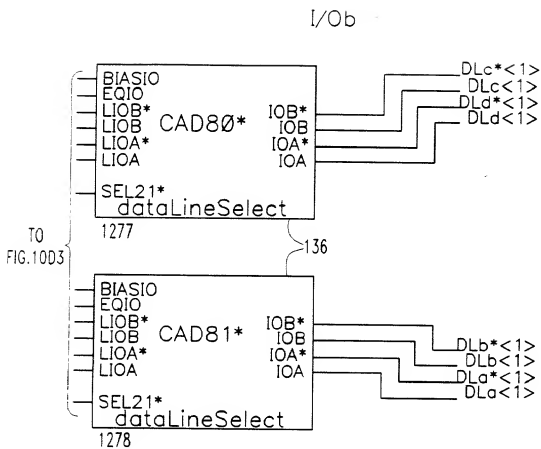


FIG. 10D4

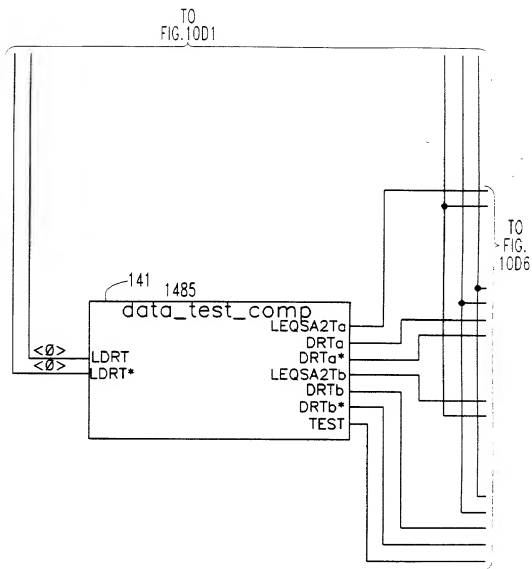


FIG. 10D5

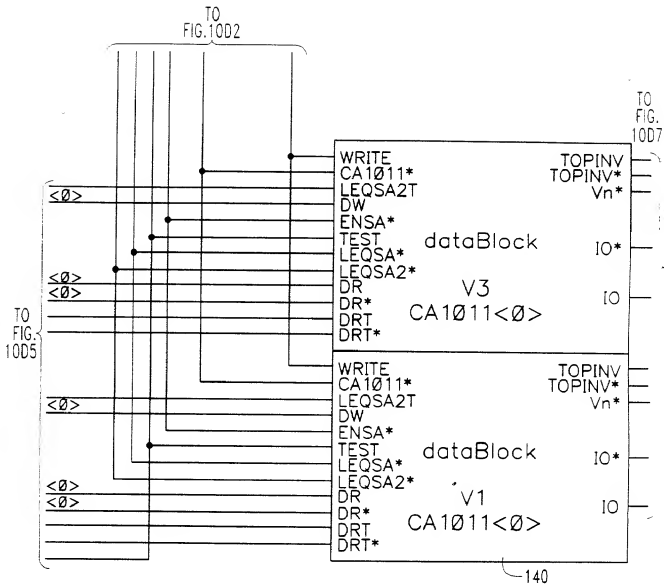


FIG. 10D6

2025 RELEASE UNDER E.O. 14176

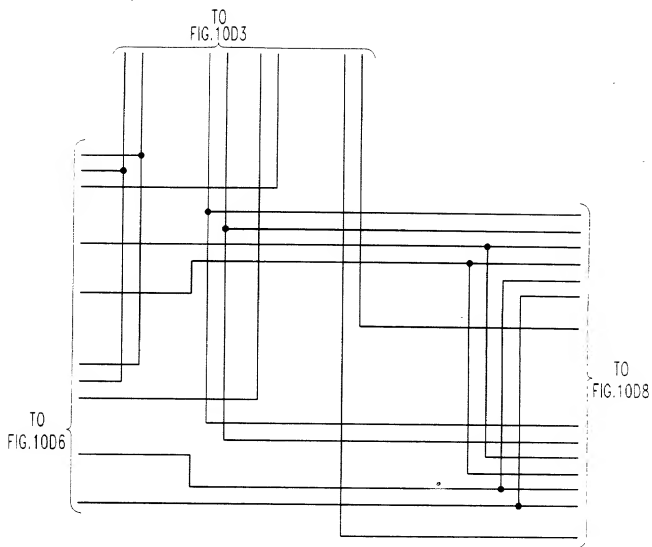


FIG. 10D7

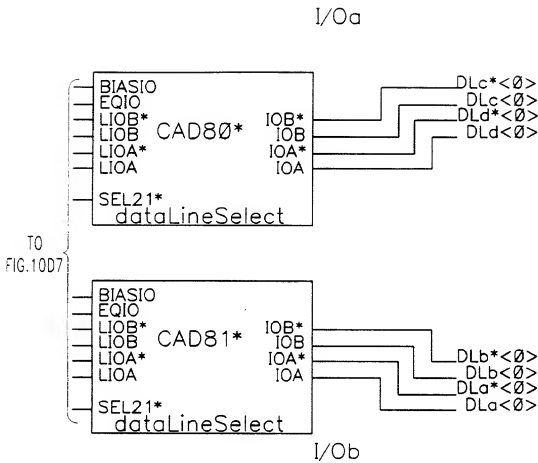


FIG.10D8

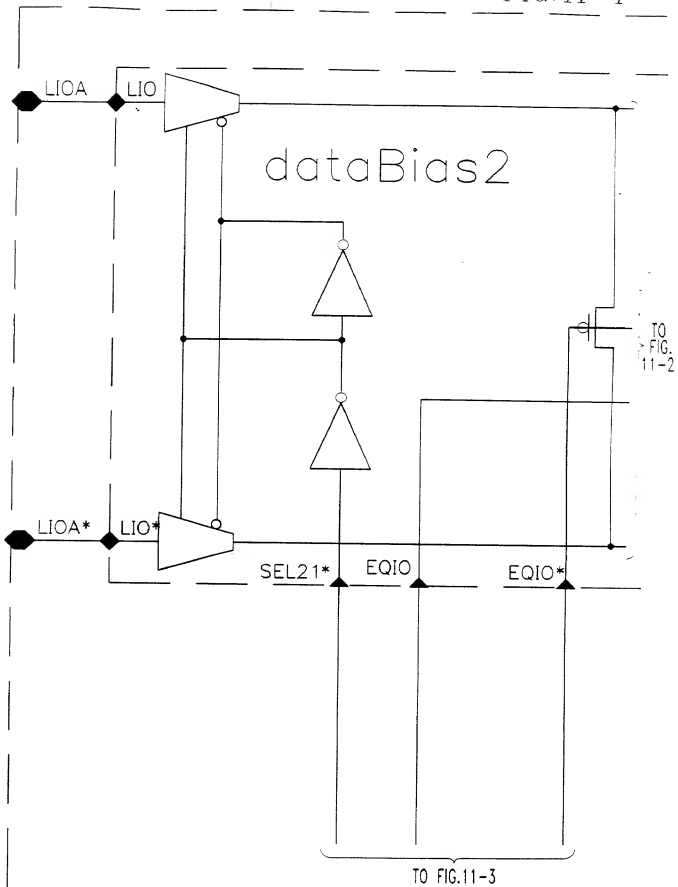
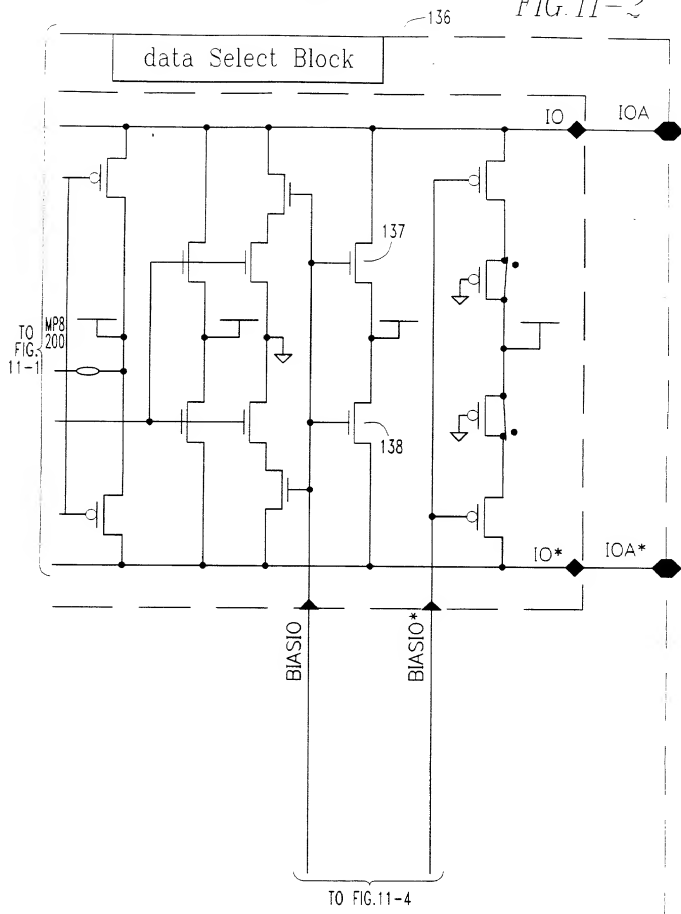


FIG. 11-2



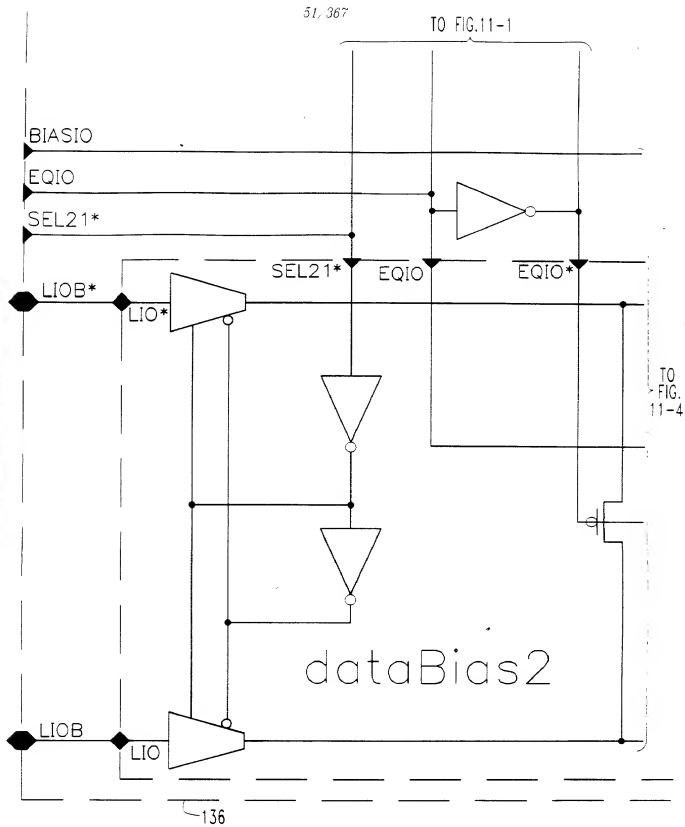


FIG. 11-3

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TO FIG. 11-2

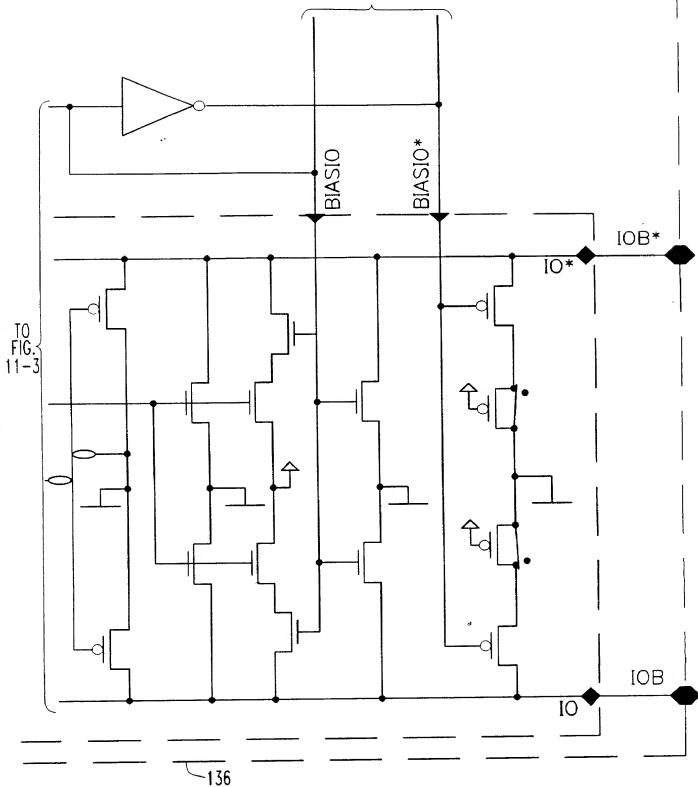
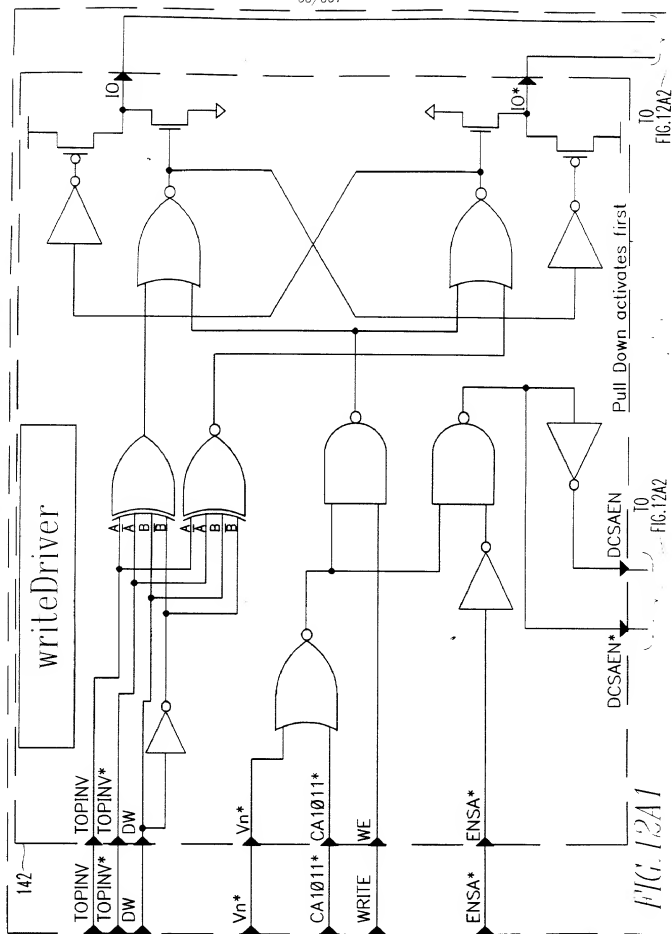


FIG. 11-4



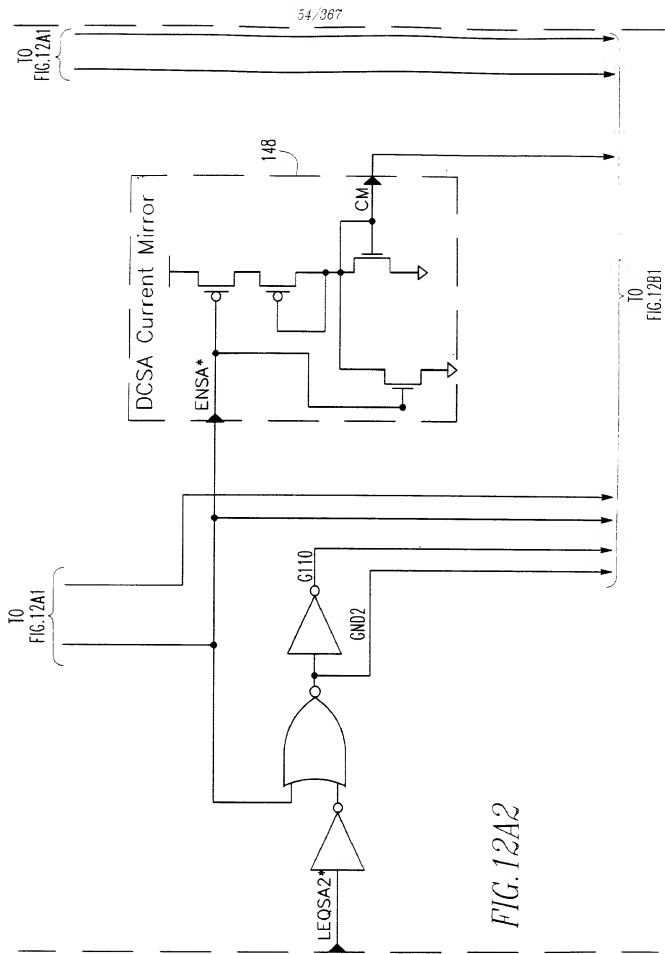


FIG. 12B1

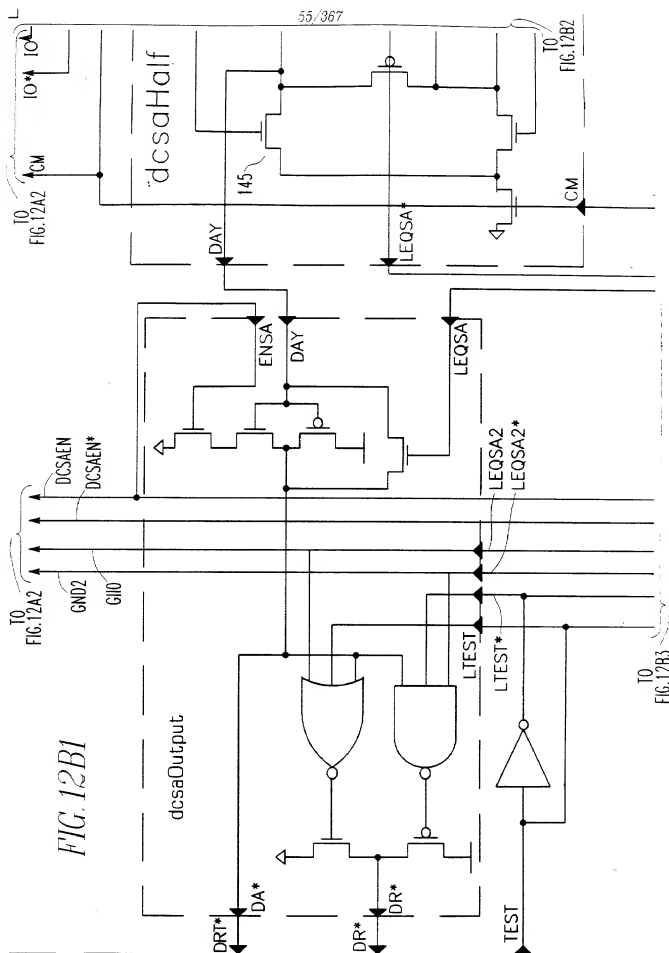


FIG. 12B3

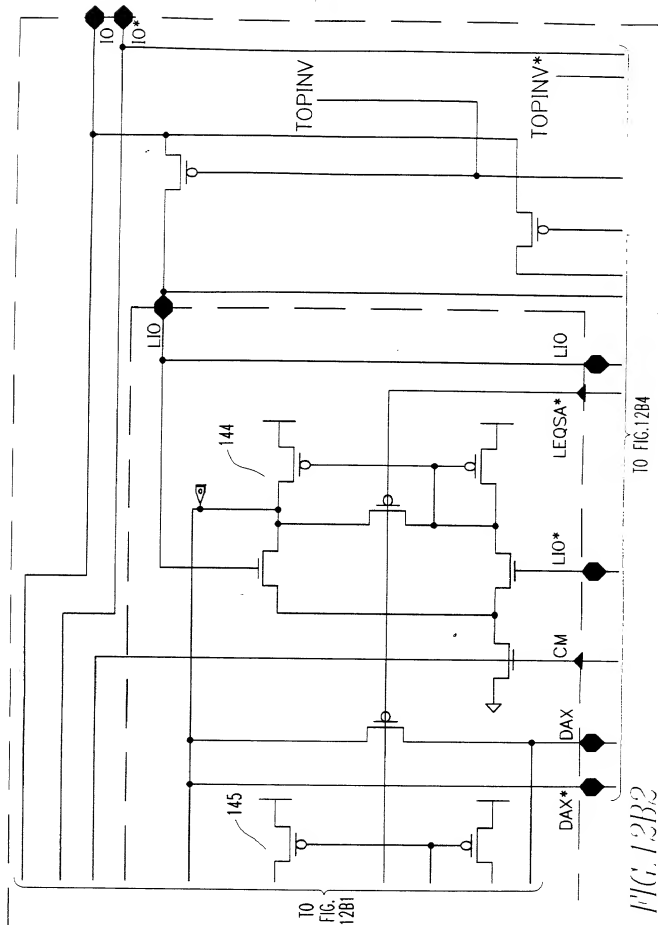
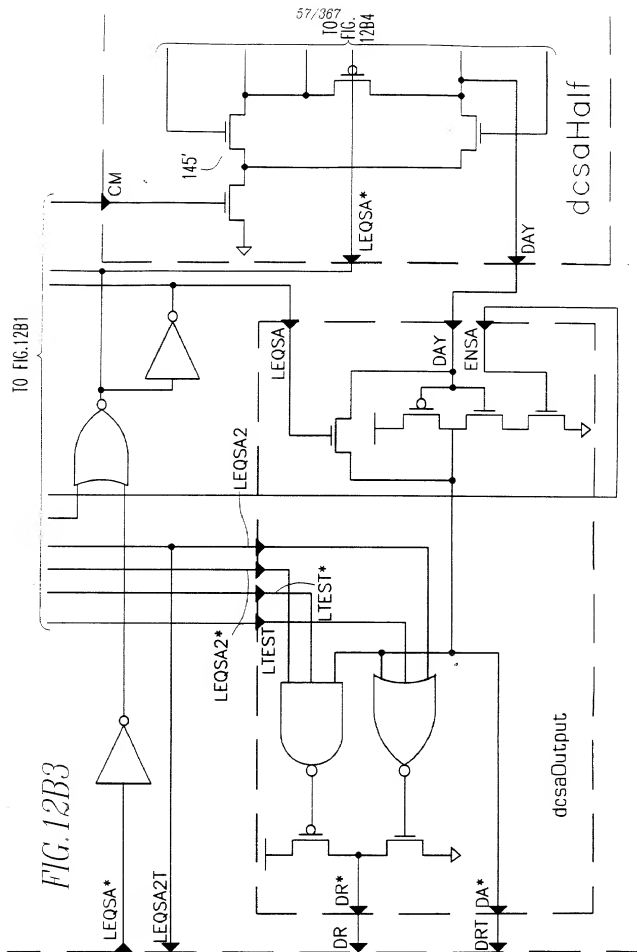
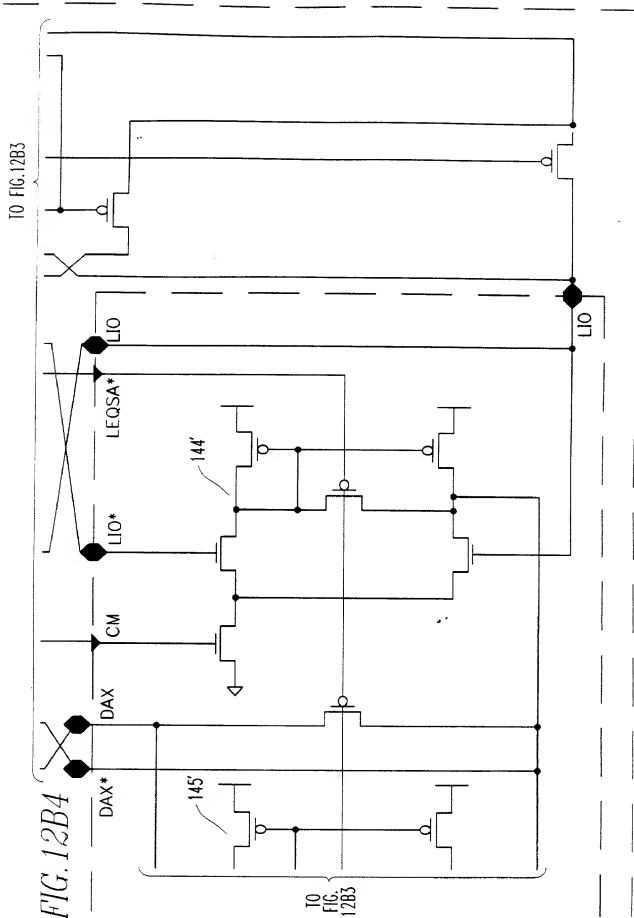


FIG. 12B3





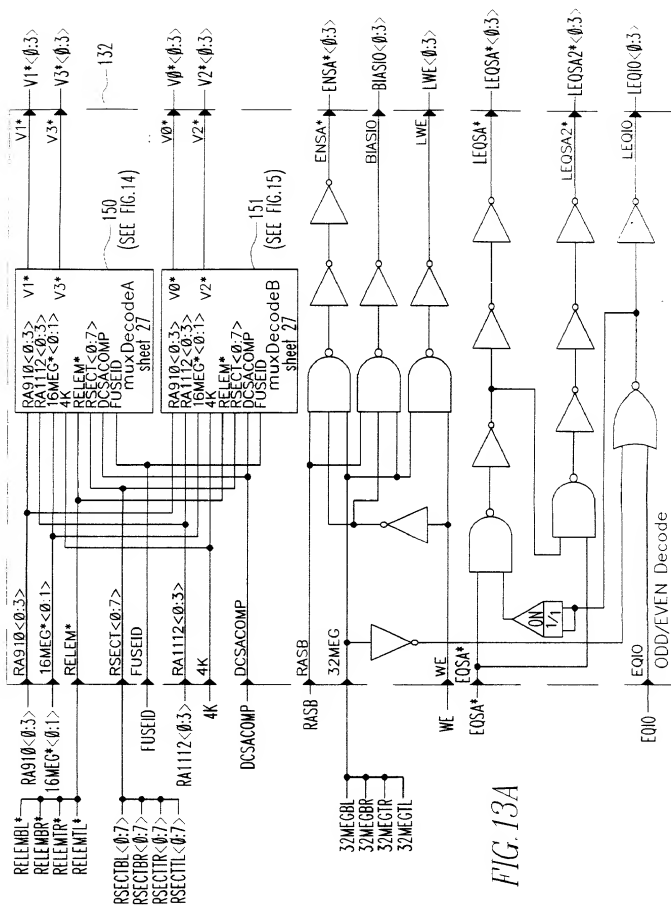


FIG. 13A

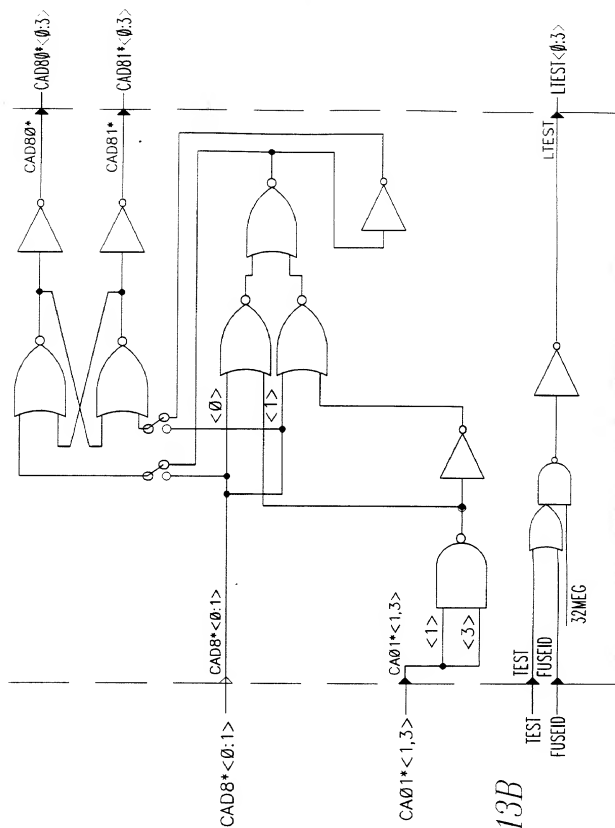


FIG 13B

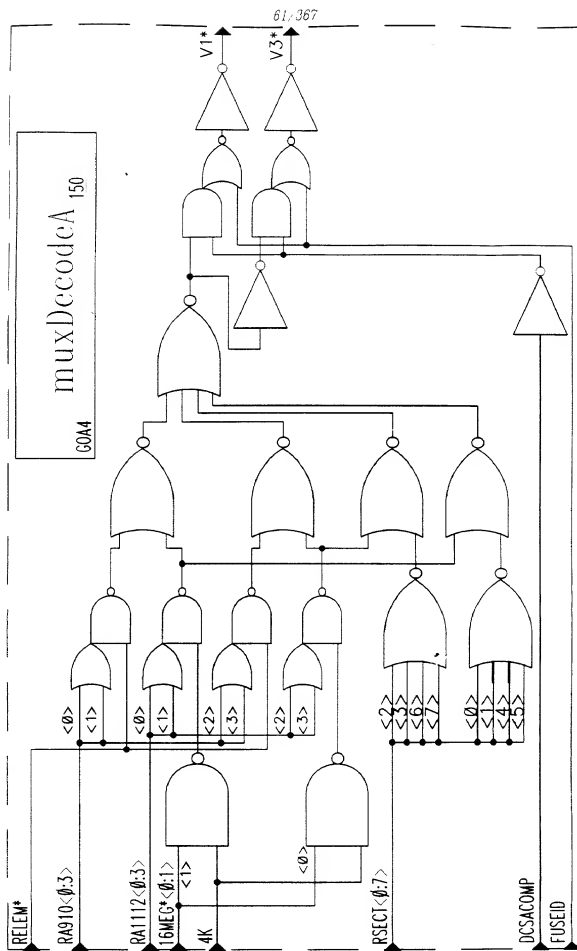


FIG. 11

FIG 15-1

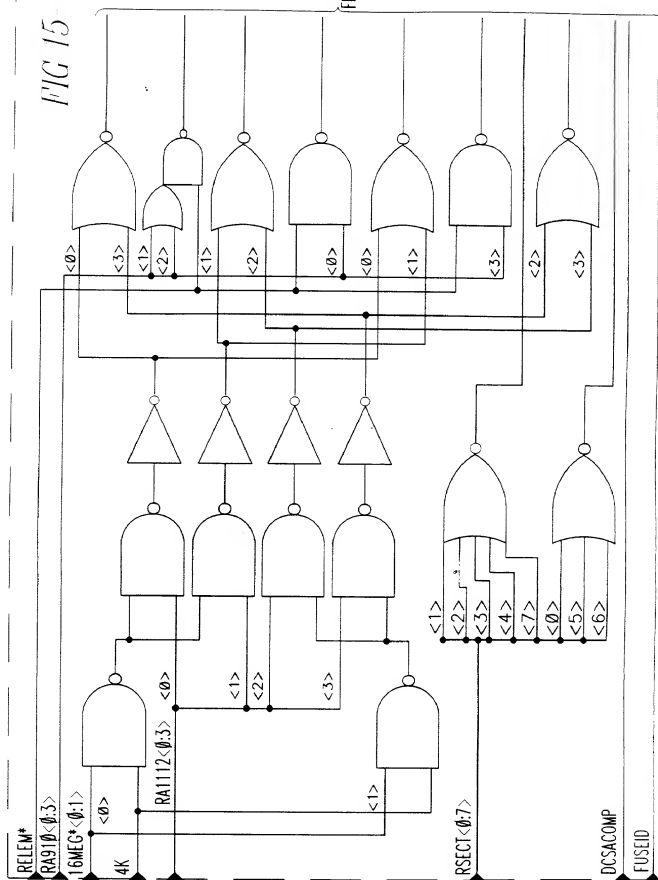


FIG. 15--2

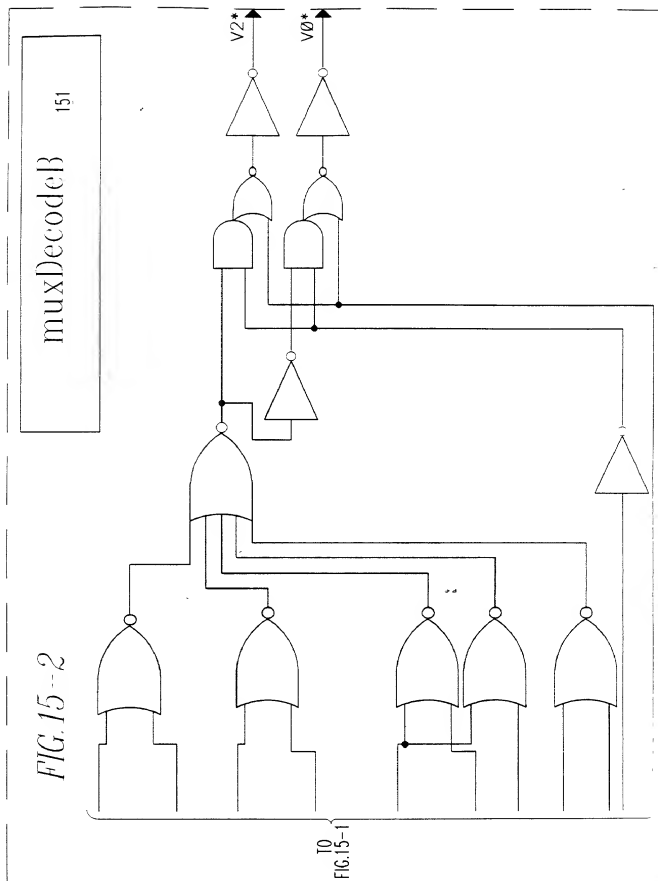
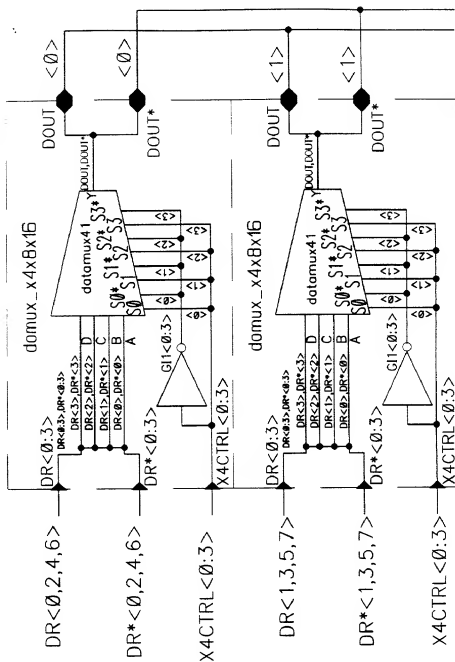
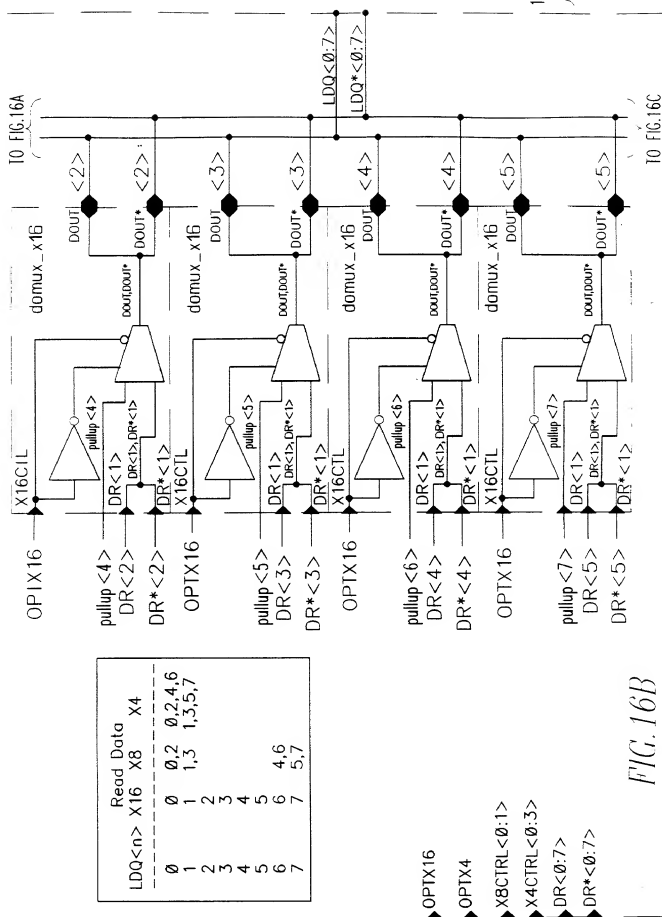
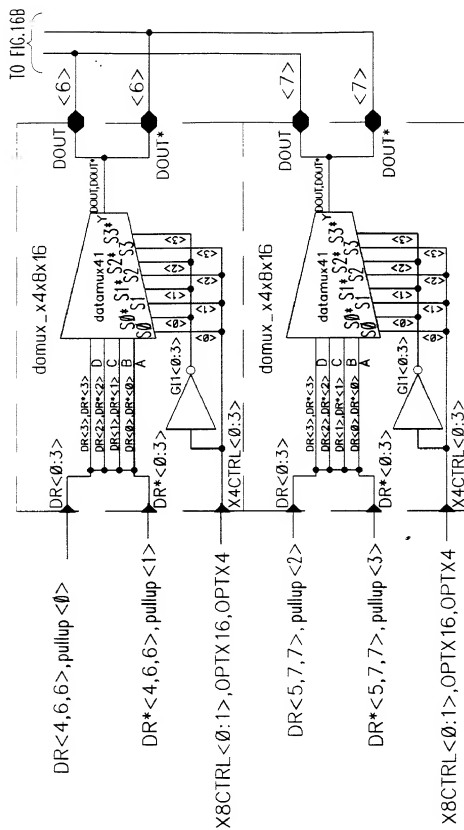


FIG. 16A



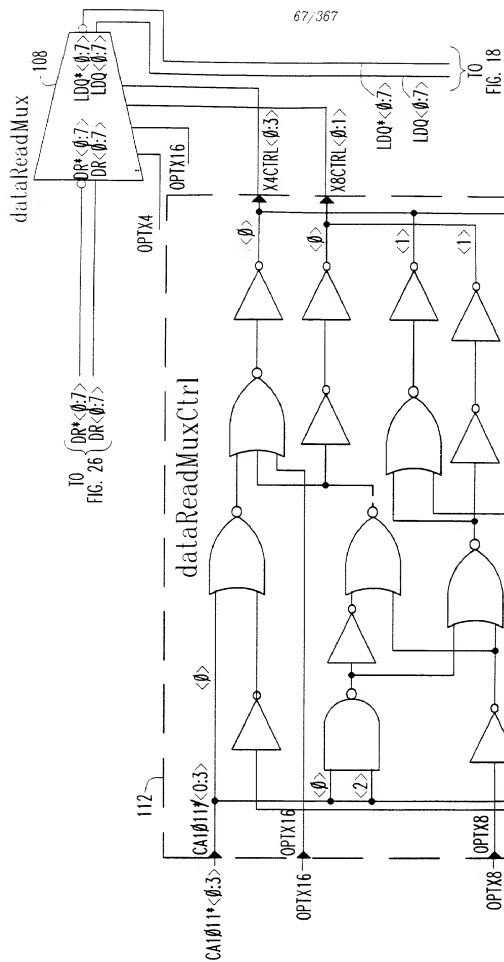




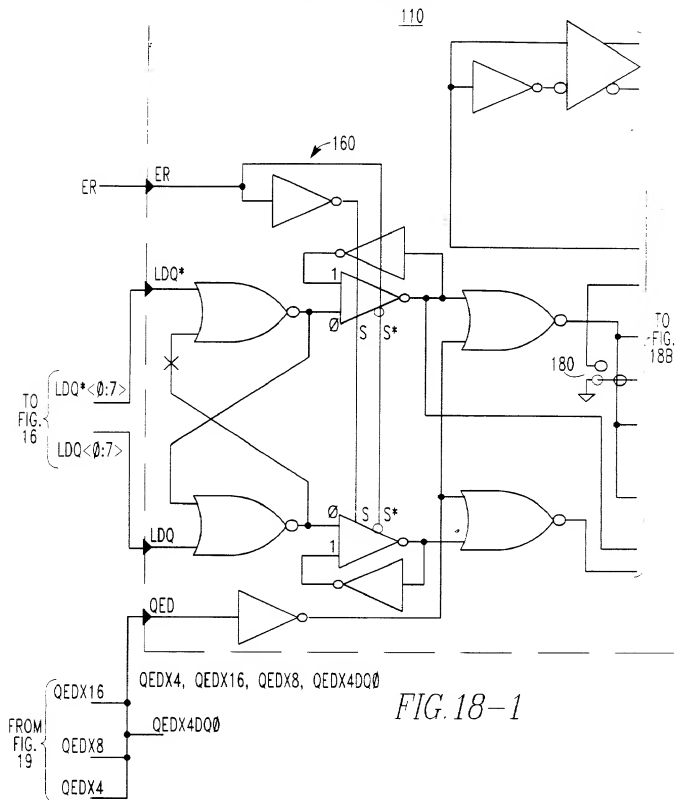
T.W. pullup <0:7>

dataReadMux

FIG. 16C



DATA OUTPUT BUFFER



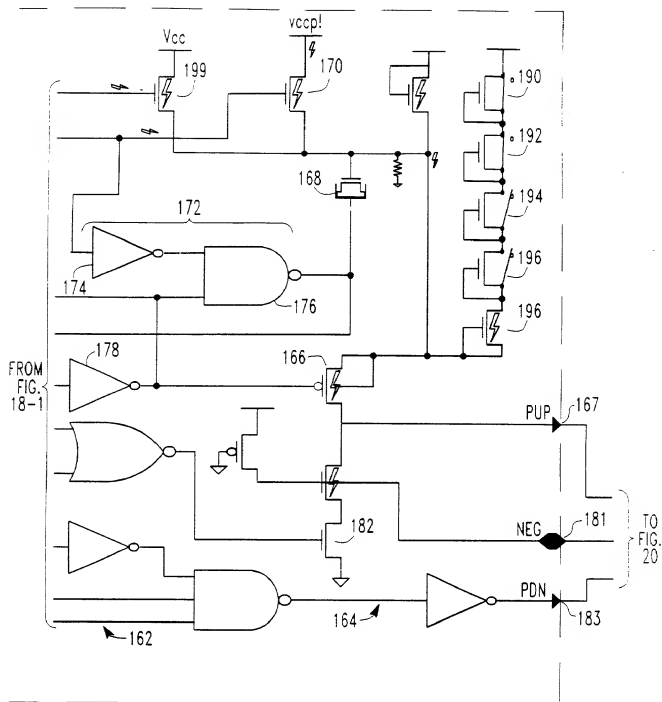


FIG. 18-2

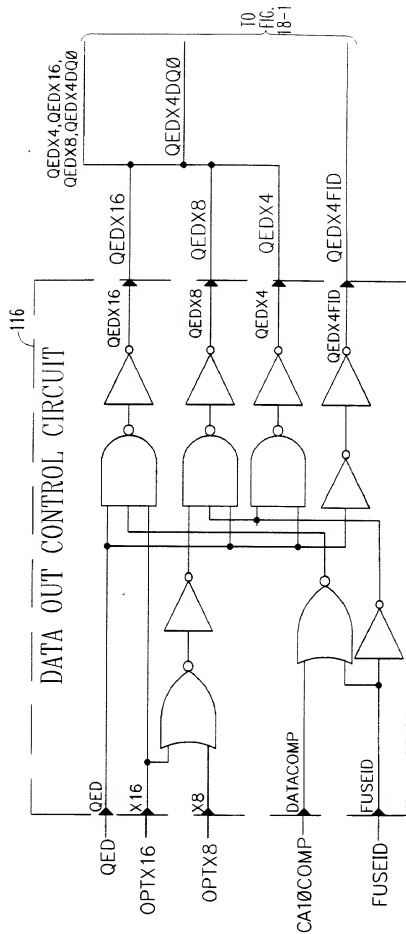


FIG. 19

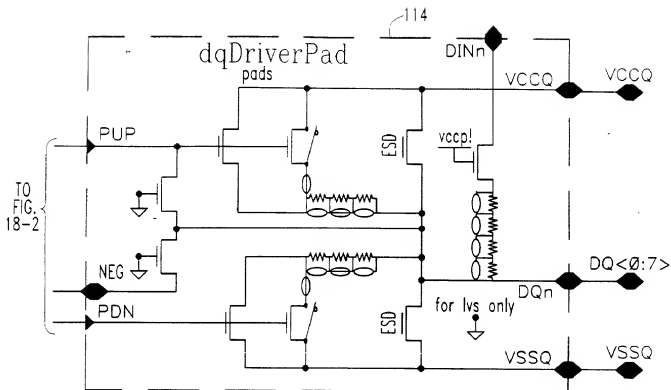


FIG. 20

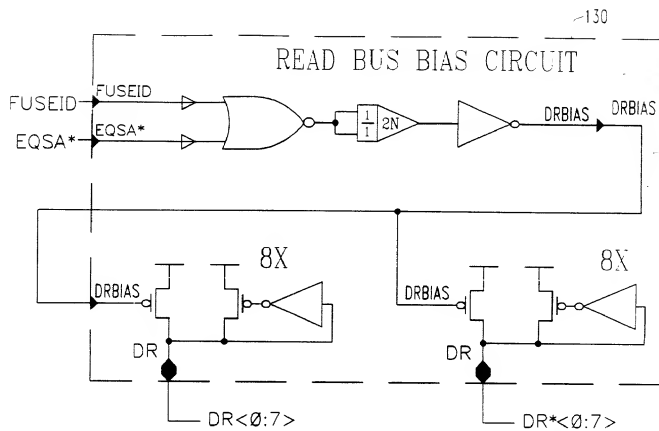


FIG. 21

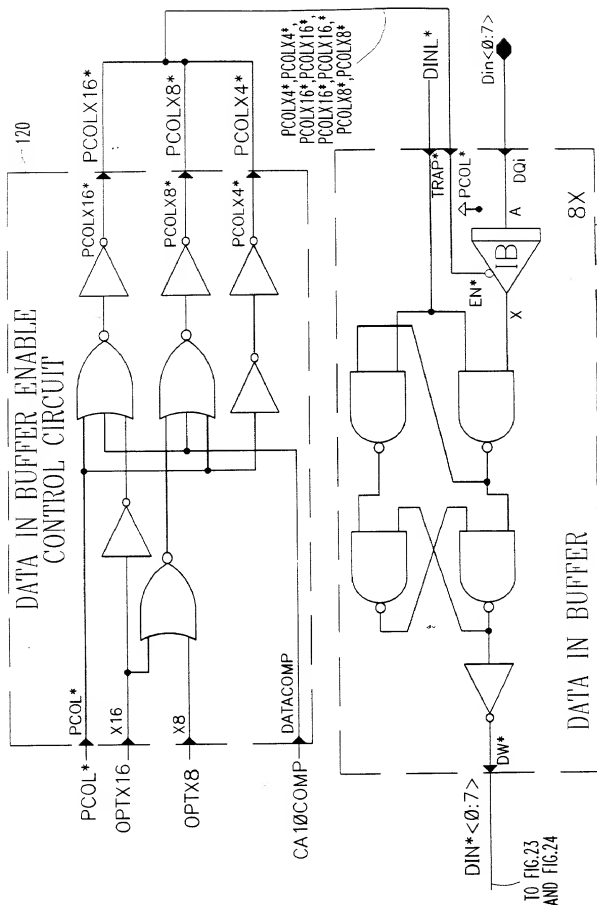
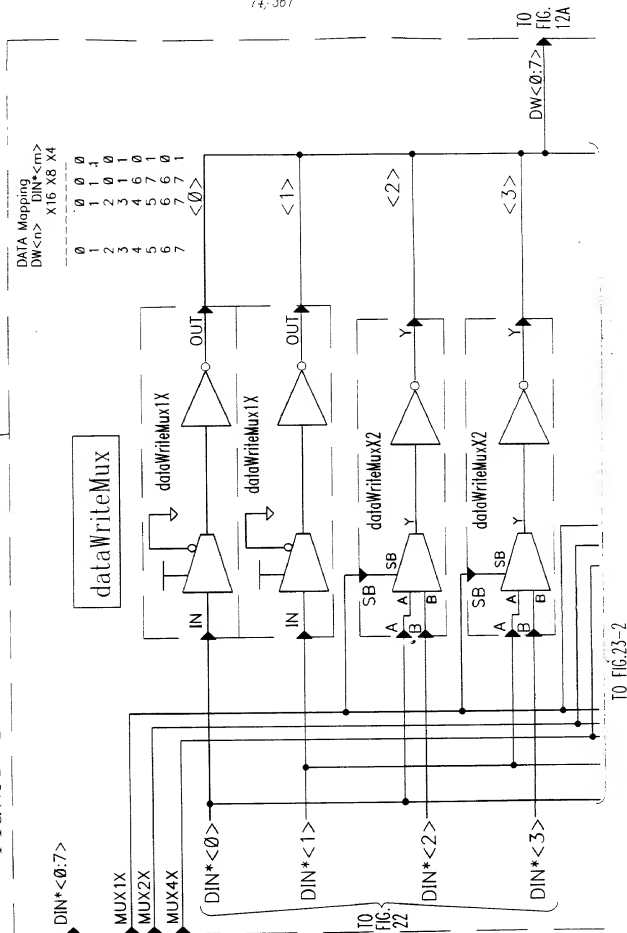


FIG. 23-1

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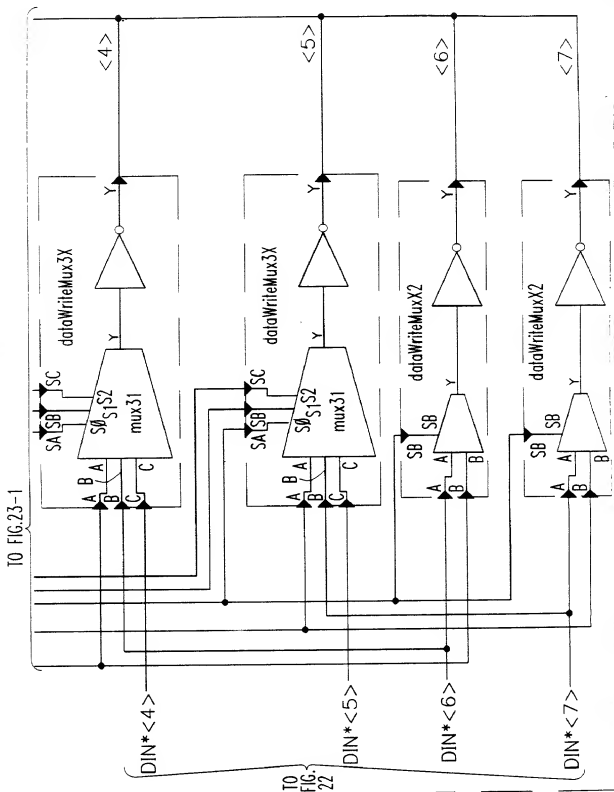


FIG. 23-2

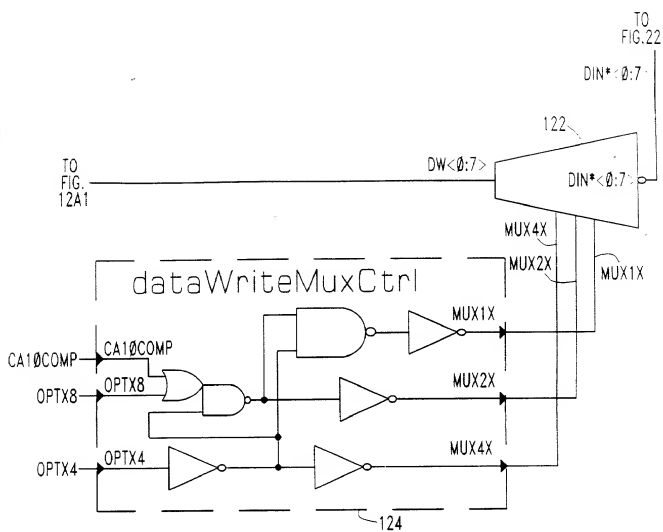


FIG. 24

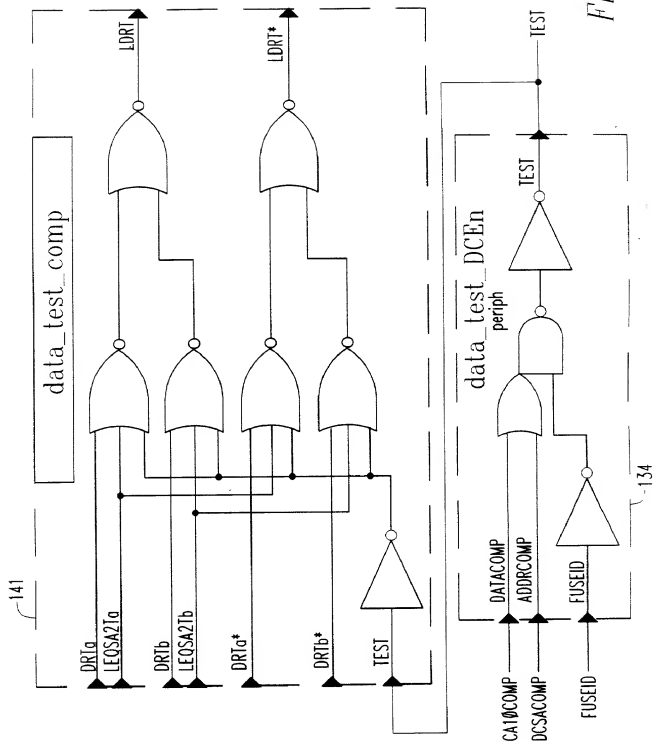


FIG. 25

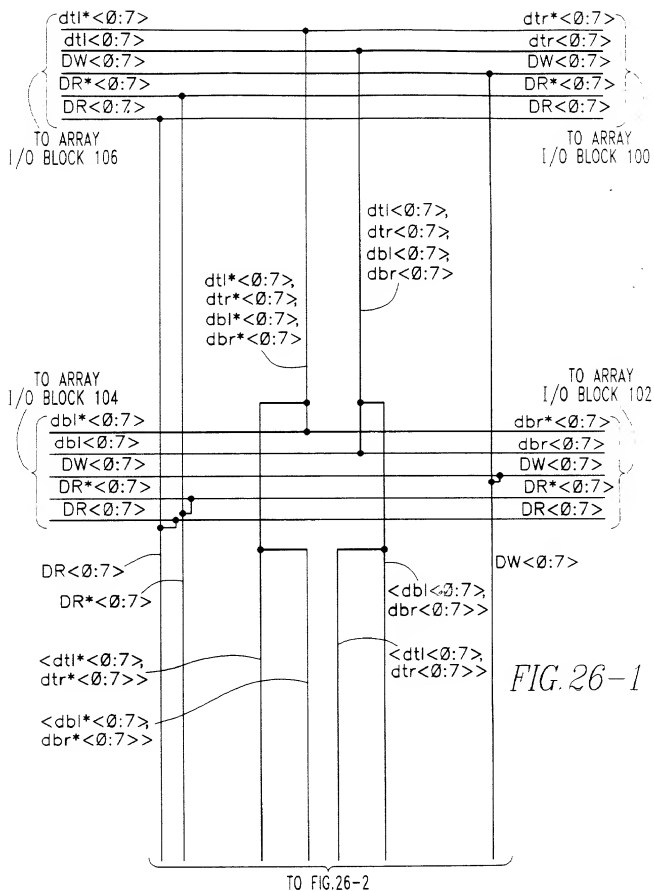


FIG. 26-1

FROM FIG. 26-1

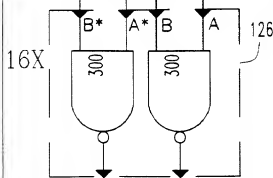
READ/WRITE
BUS $tdl^* < 0:7 >$,
 $tdr^* < 0:7 >$ $tdl < 0:7 >$ $tdl < 0:7 >$,
 $tdr < 0:7 >$ $tdr^* < 0:7 >$ $tdr < 0:7 >$ $tdl^* < 0:7 >$ $TDL^* < 0:7 >$
 $TDL < 0:7 >$ $TDR^* < 0:7 >$
 $TDR < 0:7 >$

128 (SEE FIG. 27)

TEST

CA10COMP

datapathtest

 $DR < 0:7 >$ $DR^* < 0:7 >$ TO DATA
READ MUX 108

16X

300

300

B*

A*

B

A

126

RP13 < 0:15 >

RP2 < 0:15 >

data_test

blk_b

FROM DATA
WRITE MUX 122

FIG. 26-2

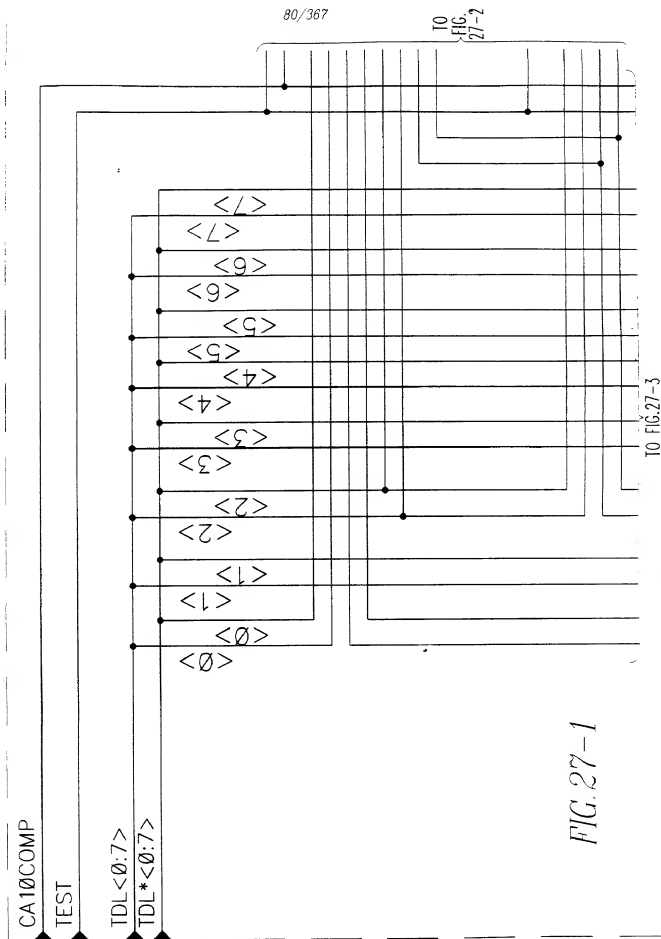
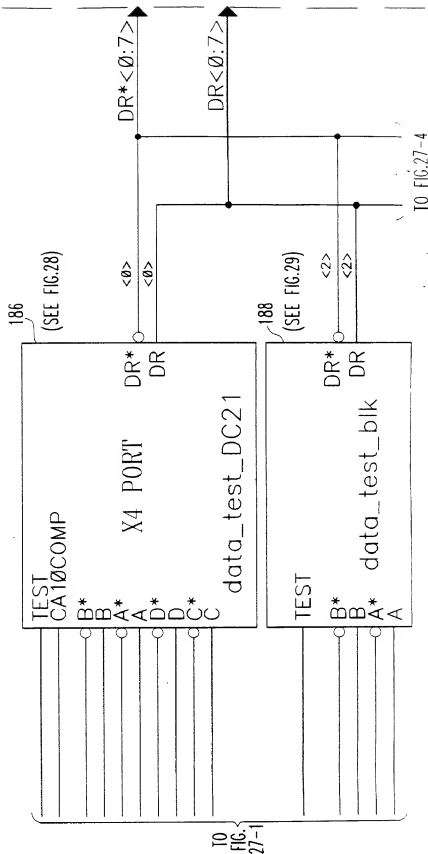


FIG. 27-2

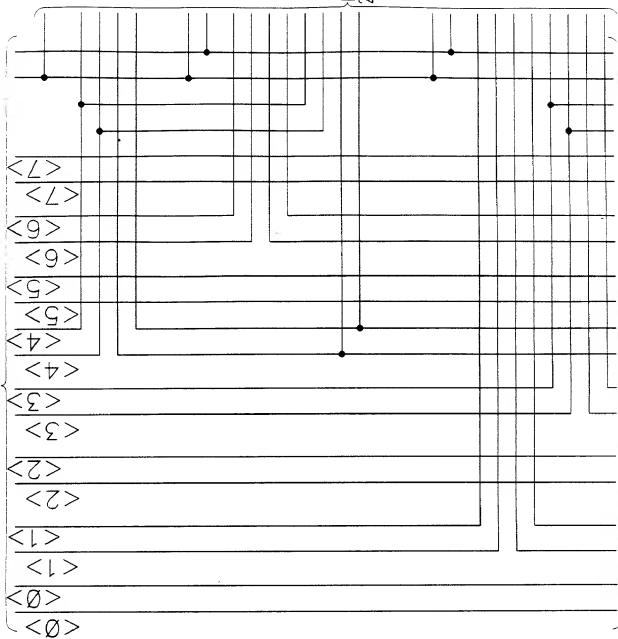
dataPathTest Block

128



TO FIG. 27-4

TO FIG. 27-1



TO FIG. 27-5

FIG. 27-3

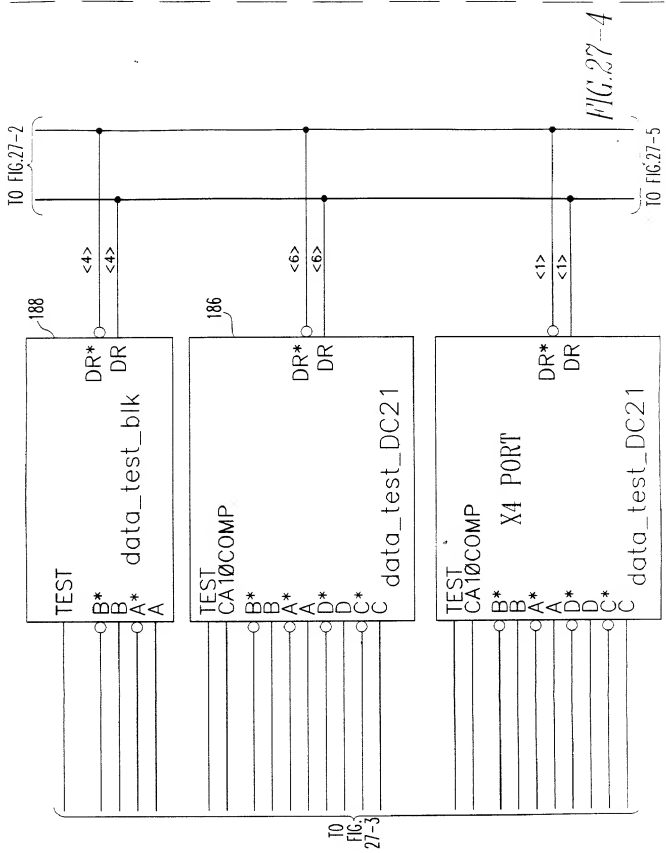
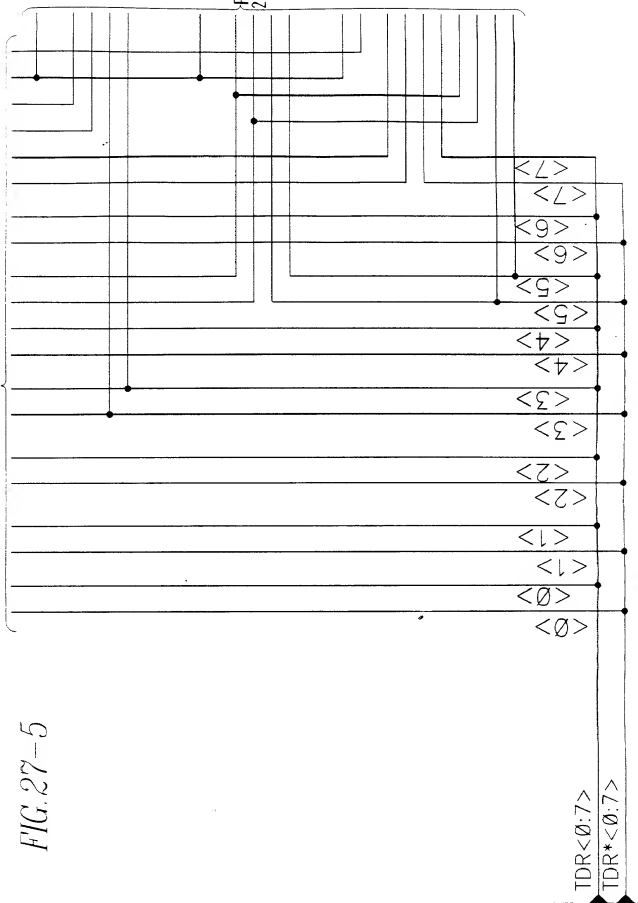


FIG. 27-4

10 FIG.27-3

FIG.27-5



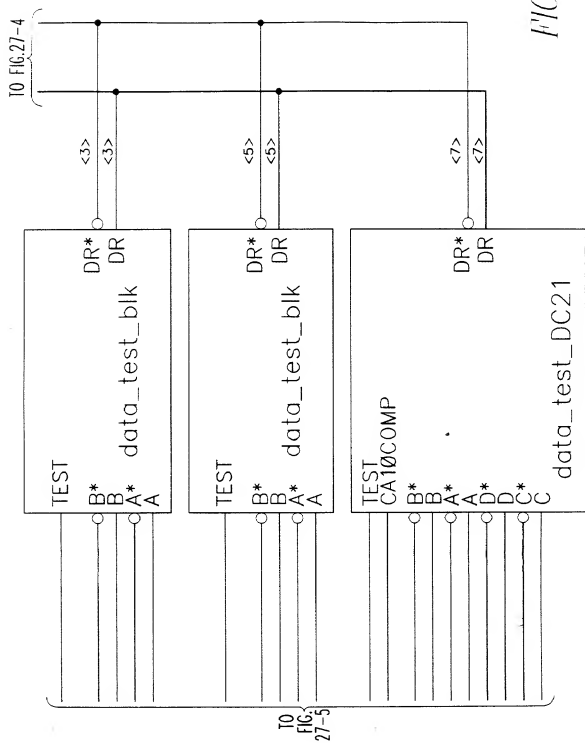


FIG. 27-6

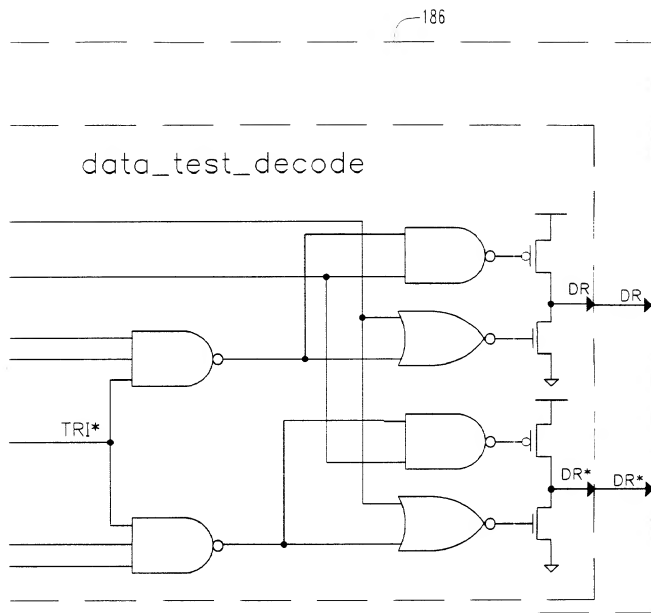


FIG. 28-2

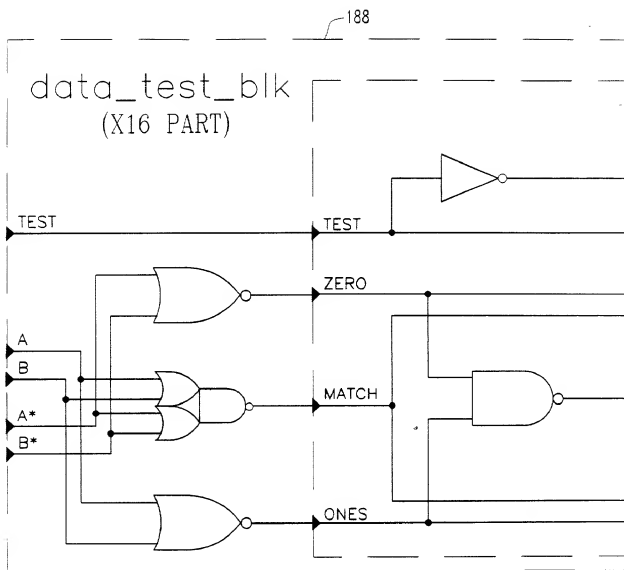


FIG. 29-1

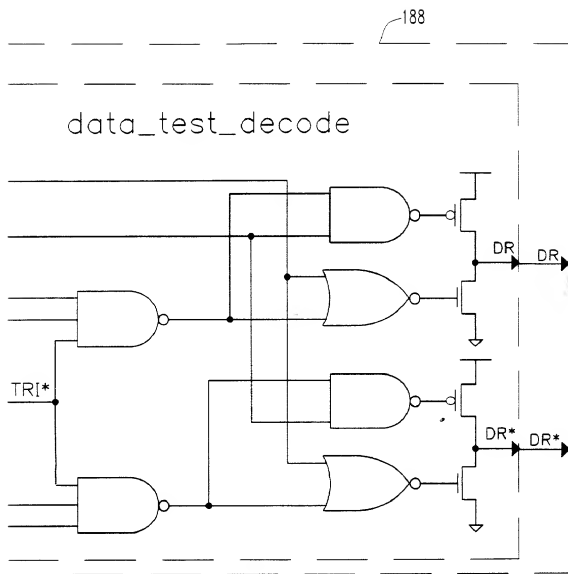


FIG. 29-2

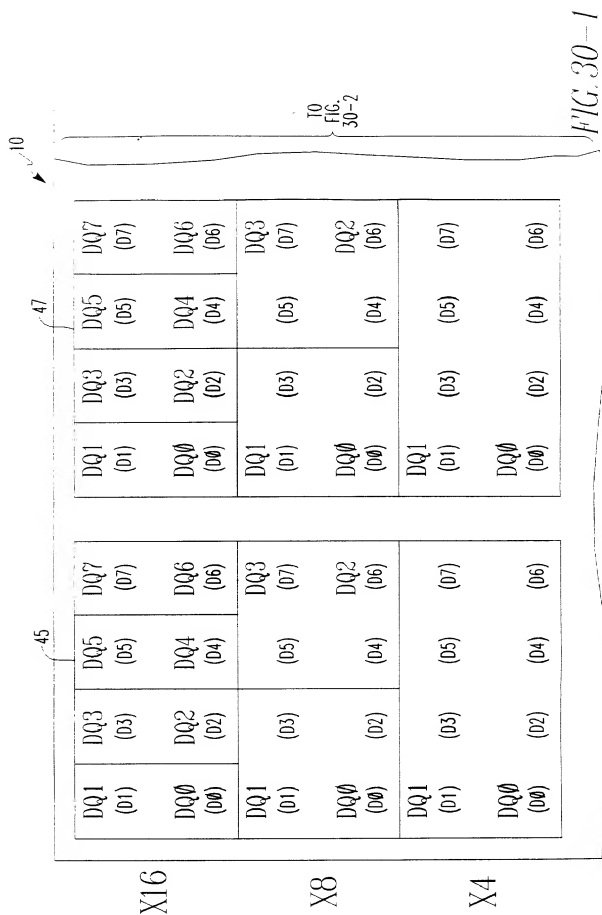
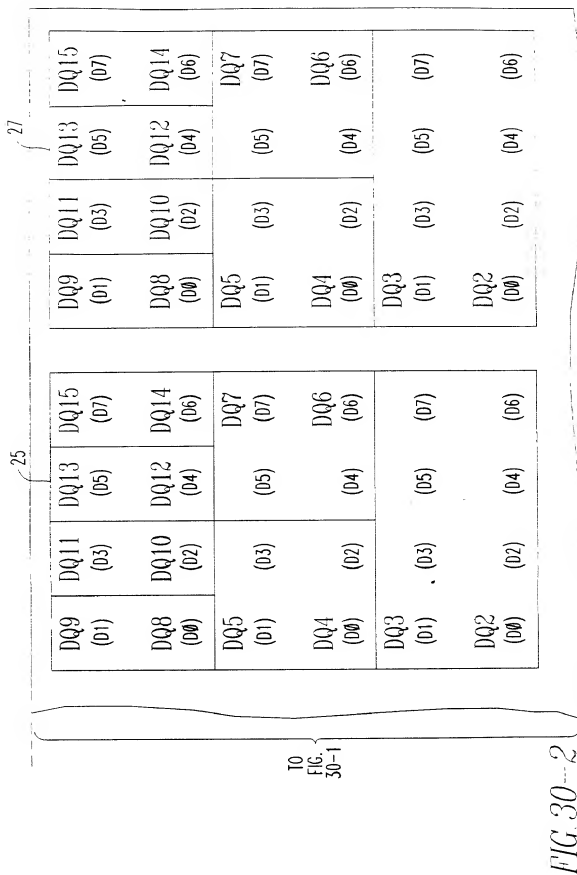


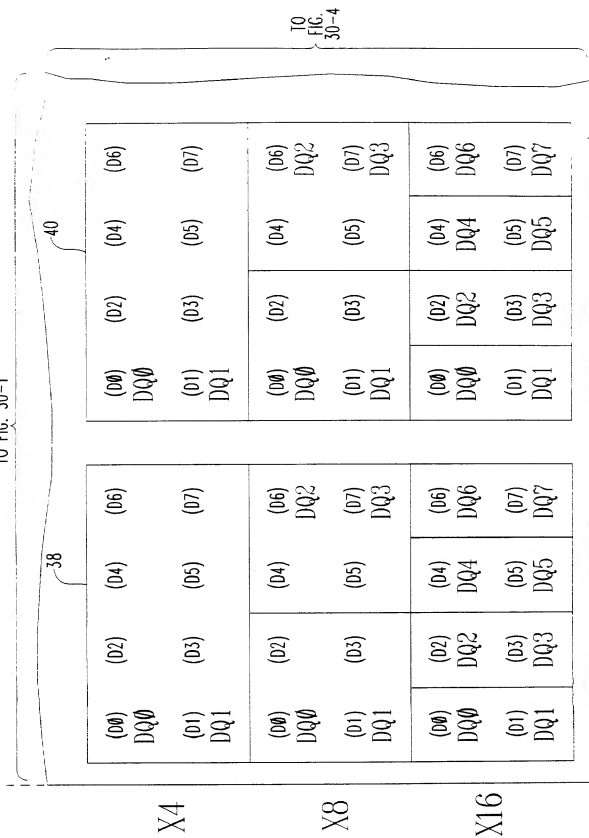
FIG. 30-3

FIG. 30-1



TO FIG. 30-4

TO FIG. 30-1



TO
FIG.
30-4

FIG. 30-3

IO FIG. 30-2

31

33

(00) DQ2	(02)	(04)	(06)
(01) DQ3	(03)	(05)	(07)
(00) DQ4	(02)	(04)	(06) DQ6
(01) DQ5	(03)	(05)	(07) DQ7
(00) DQ8	(02) DQ10	(04) DQ12	(06) DQ14
(01) DQ9	(03) DQ11	(05) DQ13	(07) DQ15

(00) DQ2	(02)	(04)	(06)
(01) DQ3	(03)	(05)	(07)
(00) DQ4	(02)	(04)	(06) DQ6
(01) DQ5	(03)	(05)	(07) DQ7
(00) DQ8	(02) DQ10	(04) DQ12	(06) DQ14
(01) DQ9	(03) DQ11	(05) DQ13	(07) DQ15

IO
FIG.
30-3

FIG 30-4

X4	VSSQ	N/C	VSSQ	N/C	N/C	N/C
X8	VSSQ	DQ3	VSSQ	DQ2	N/C	N/C
X16	VSSQ	DQ7	VSSQ	DQ6	DQ5	DQ5
	1	2	3	4	5	6
	7	8	9	10	11	12
X16	VCCQ	DQ0	VCCQ	DQ1	DQ2	VCCQ
X8	VCCQ	DQ0	VCCQ	DQ1	N/C	N/C
X4	VCCQ	DQ0	VCCQ	DQ1	N/C	N/C

FIG. 31A1

TO FIG. 31A2

TO FIG. 31A1

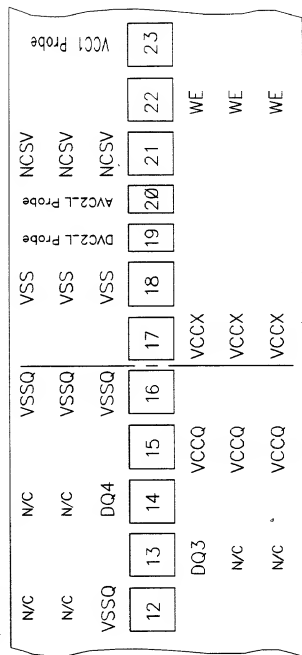
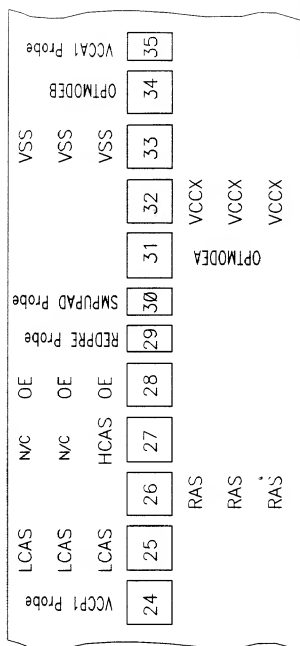


FIG. 31A2



TO FIG. 31B2

FIG. 31B1

TO FIG. 31B1

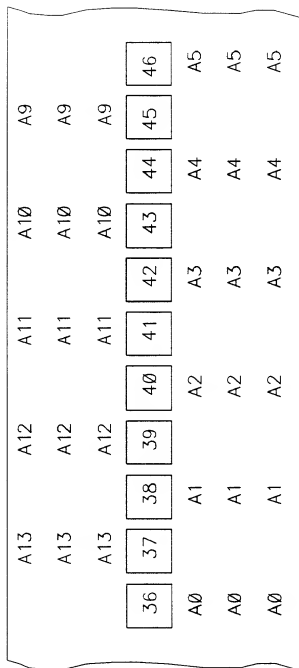


FIG. 31B2



FIG. 31C1

[illegible]

FIG. 31C2

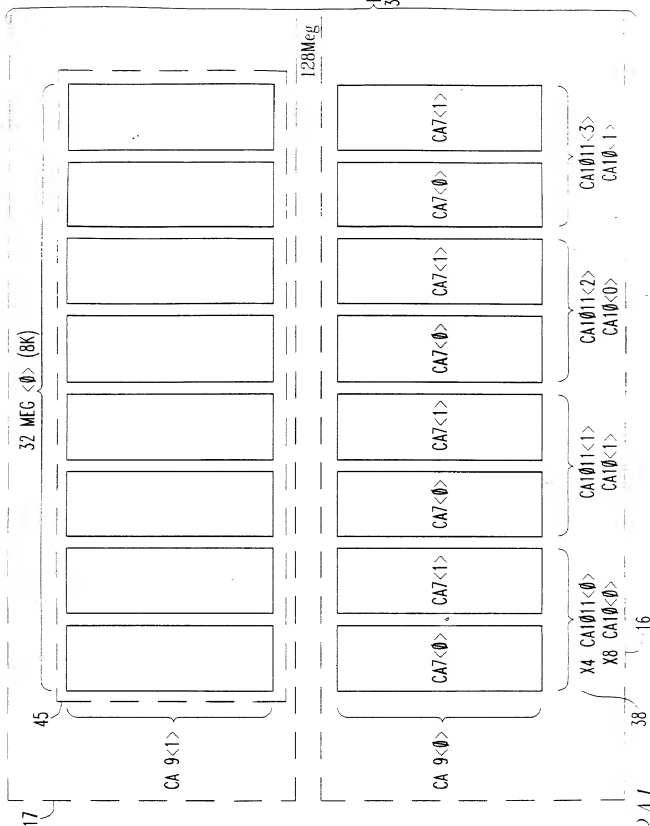
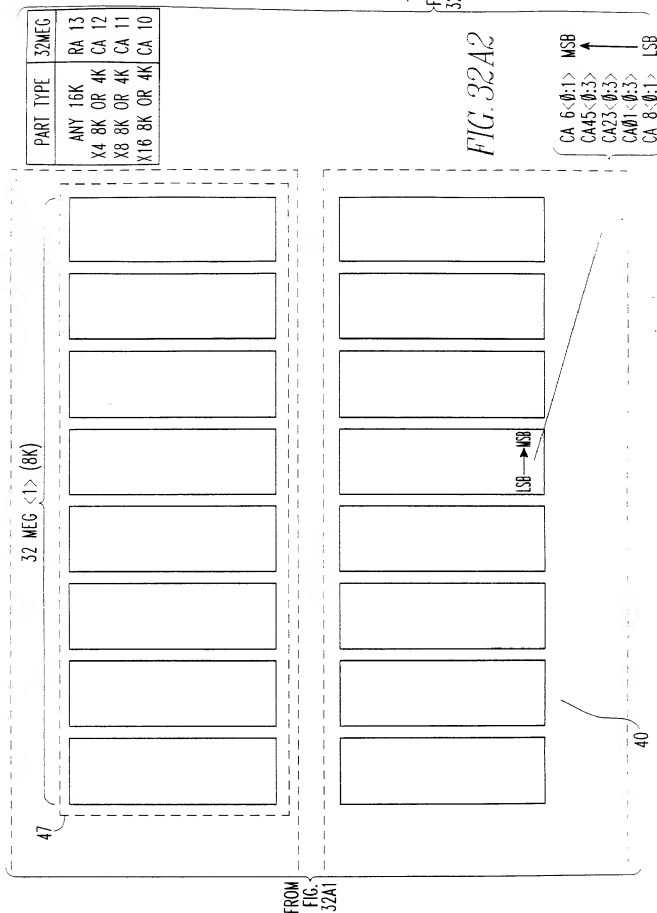
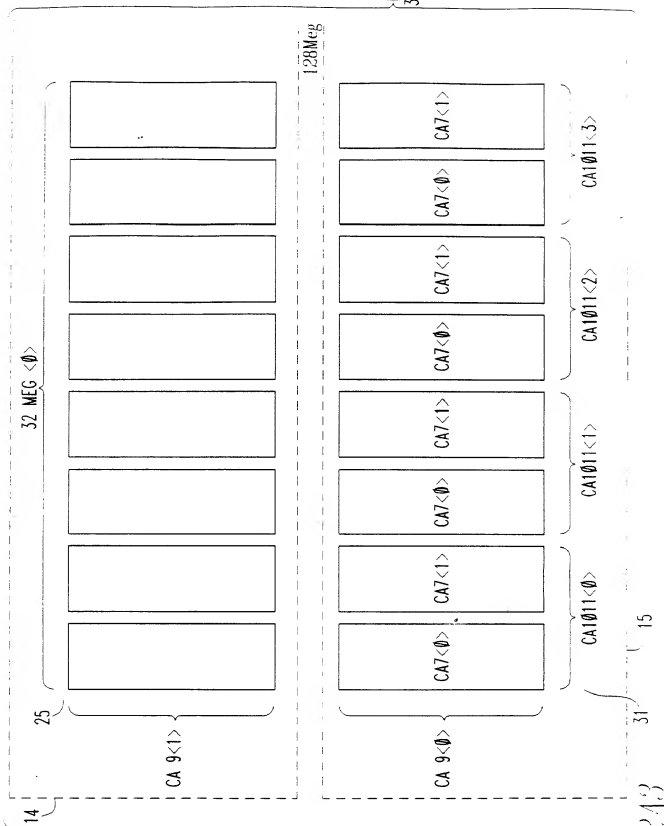
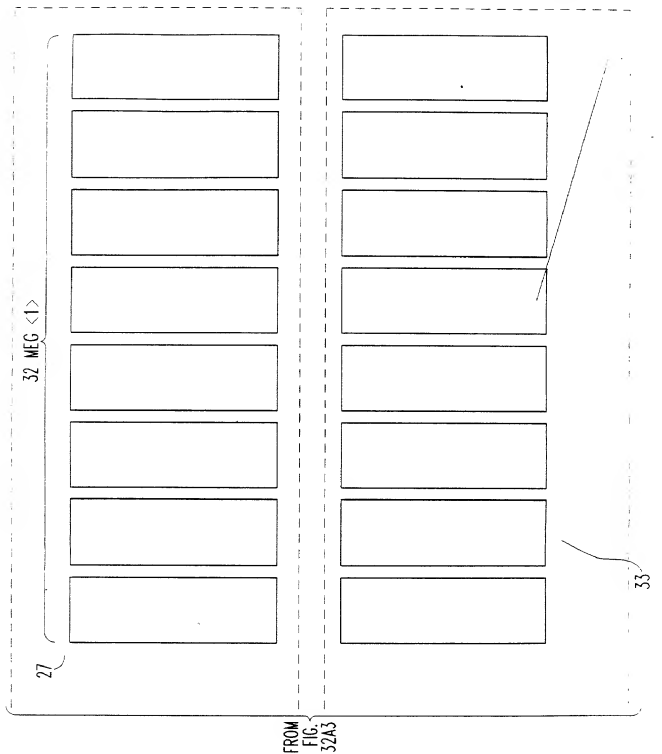


FIG. 32A1





FROM
FIG.
32A2



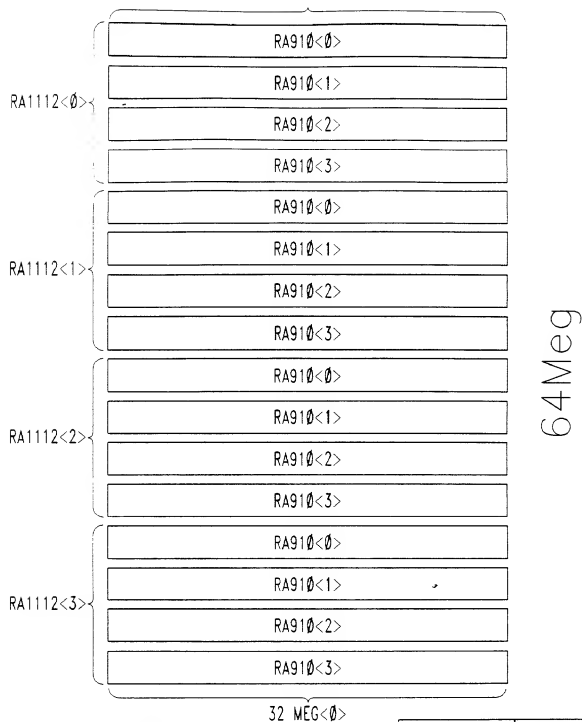


FIG. 32B1

PART TYPE	32MEG
ANY 16K	RA_13
X4 8K OR 4K	CA_12
X8 8K OR 4K	CA_11
X16 8K OR 4K	CA_10

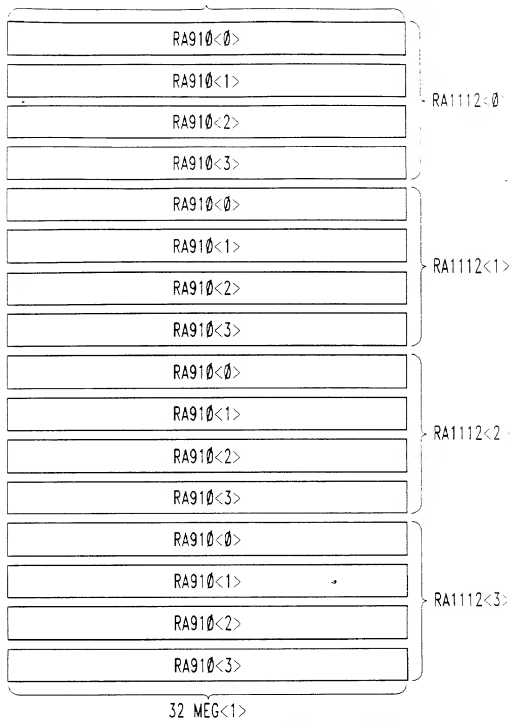


FIG. 32B2

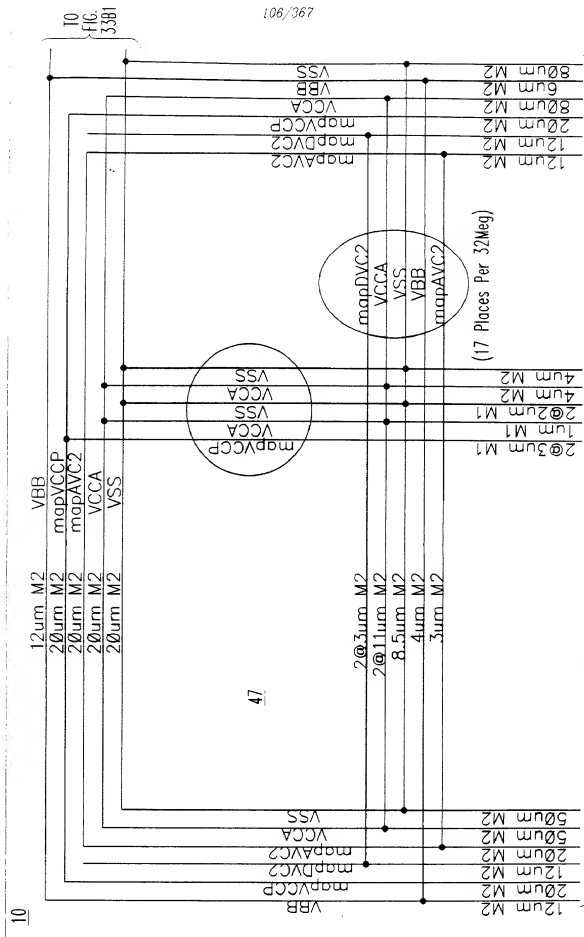
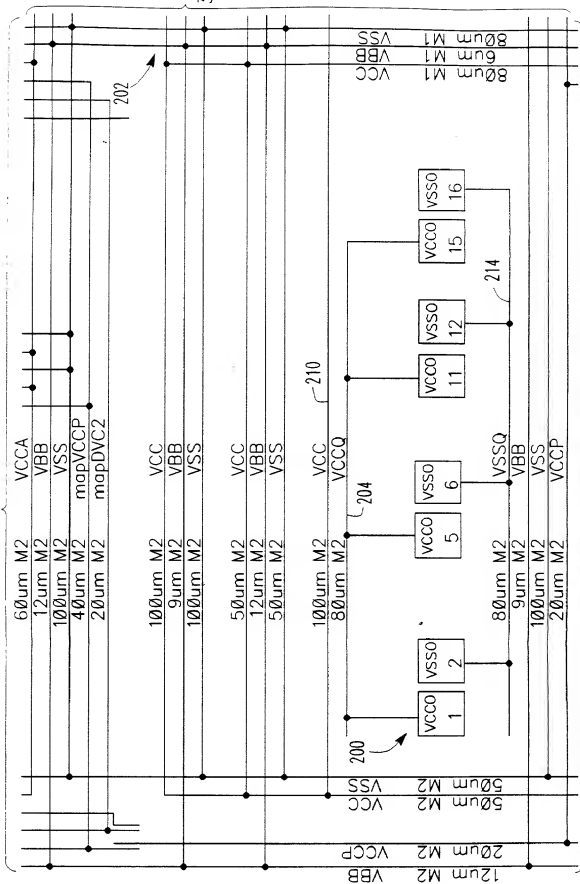


FIG. 33A2

FIG. 33A1

FROM FIG. 33A1



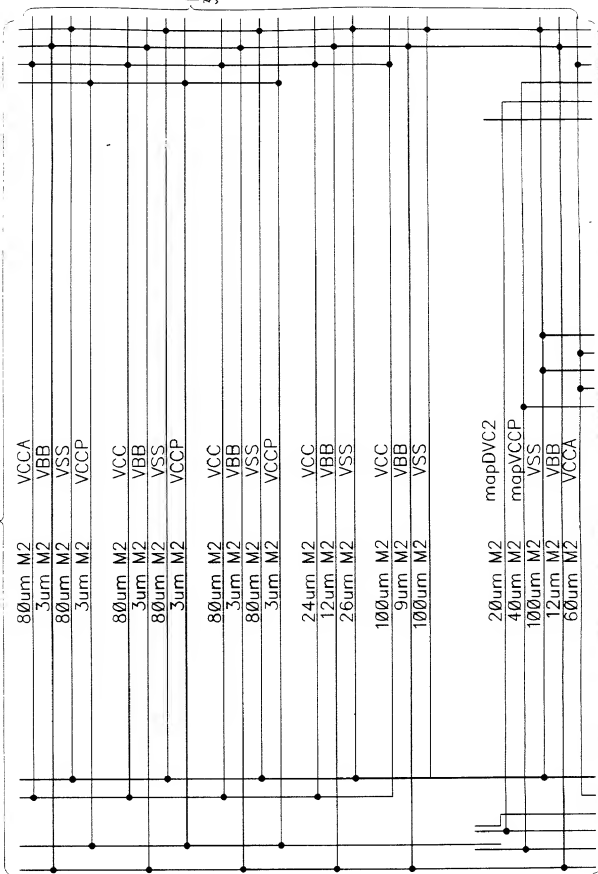
TO
FIG.
33B3

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TO FIG. 33A3

FIG. 33A2

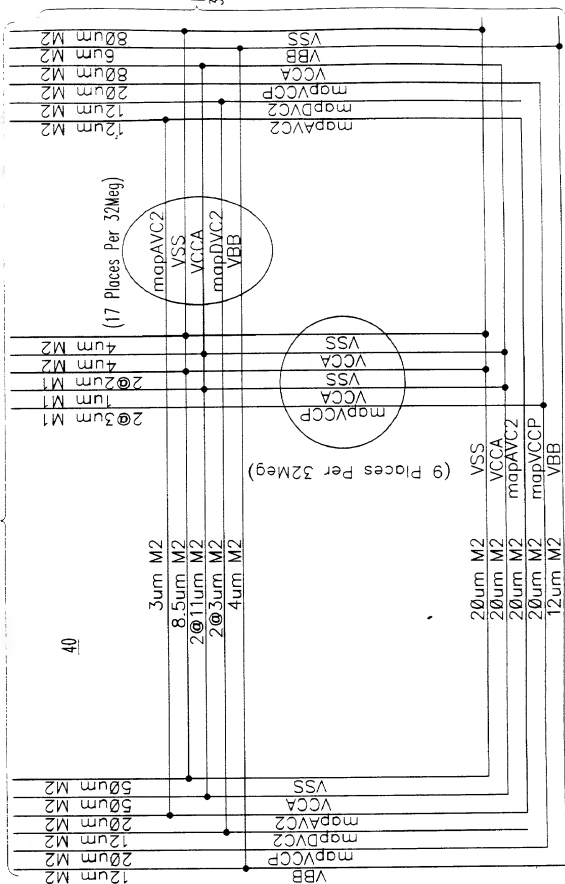
FROM FIG. 33A2



TO FIG. 33A4

FIG. 33A3

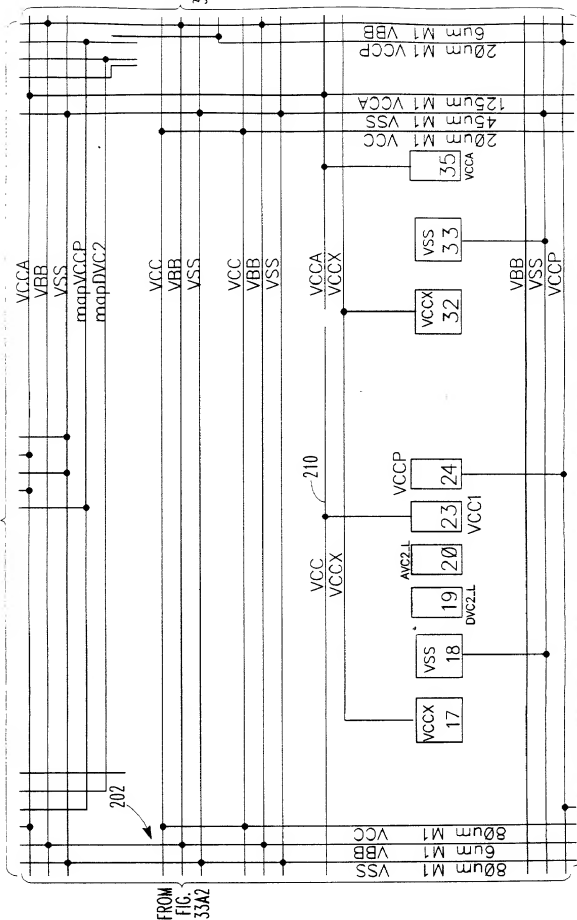
FROM FIG. 33A3



WG 33A.1


$$1/16, 1/32, 1/64$$

FROM FIG. 33B1



FROM
FIG.
33A2

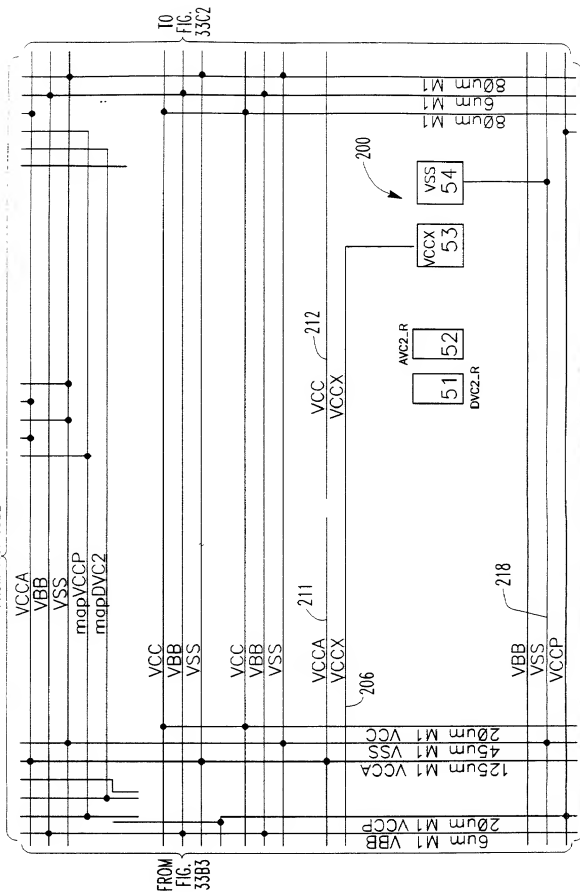
TO
FIG.
33B3

112/367

TO FIG. 33B3

FIG. 33B3

FROM FIG. 33B2



TO FIG. 33B6

FIG. 33B-1

TO
FIG.
33B6

FROM
FIG.
33A3

TO FIG. 33B7

W. G. 3335

mapDVC2
mapVCCP
VSS
VBB
VCCA

FROM FIG. 3384

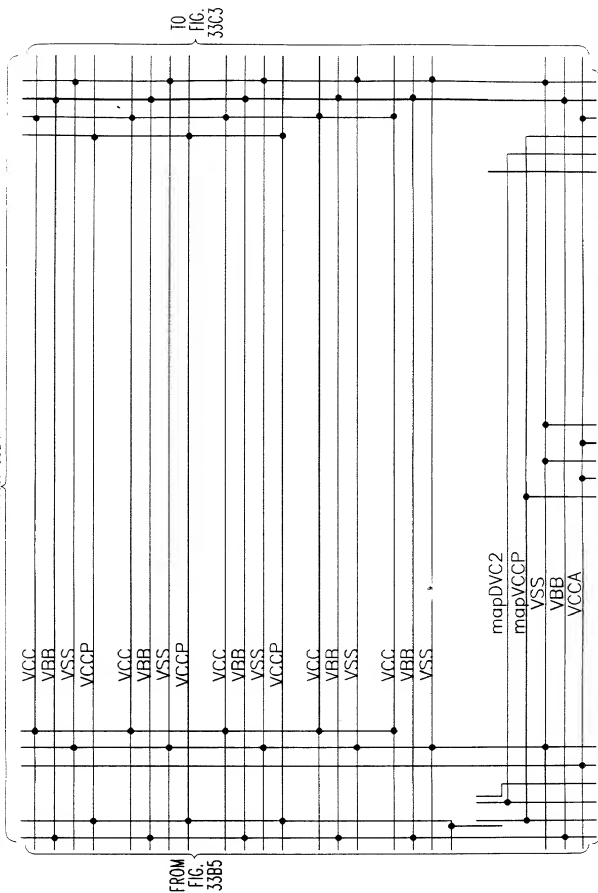


FIG. 3386

FROM FIG. 33B5

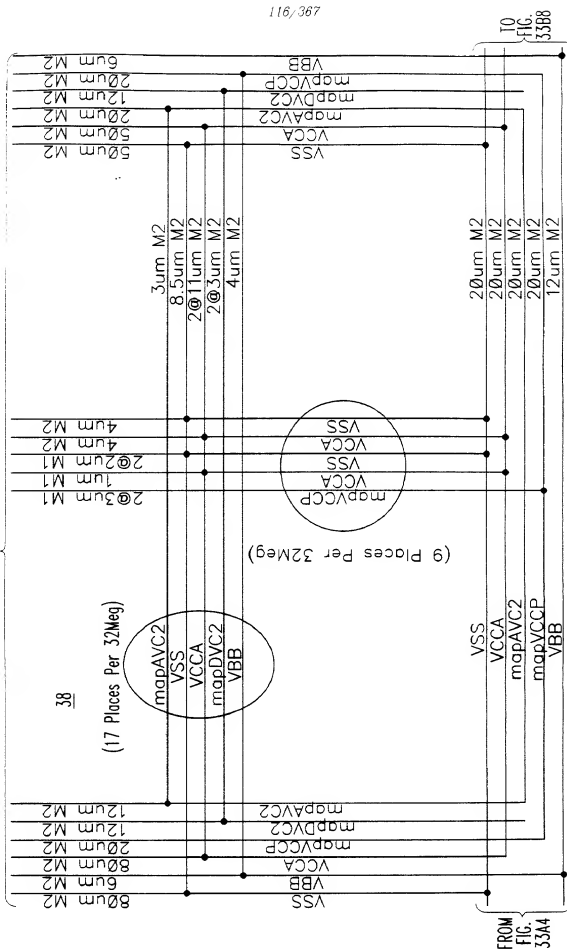
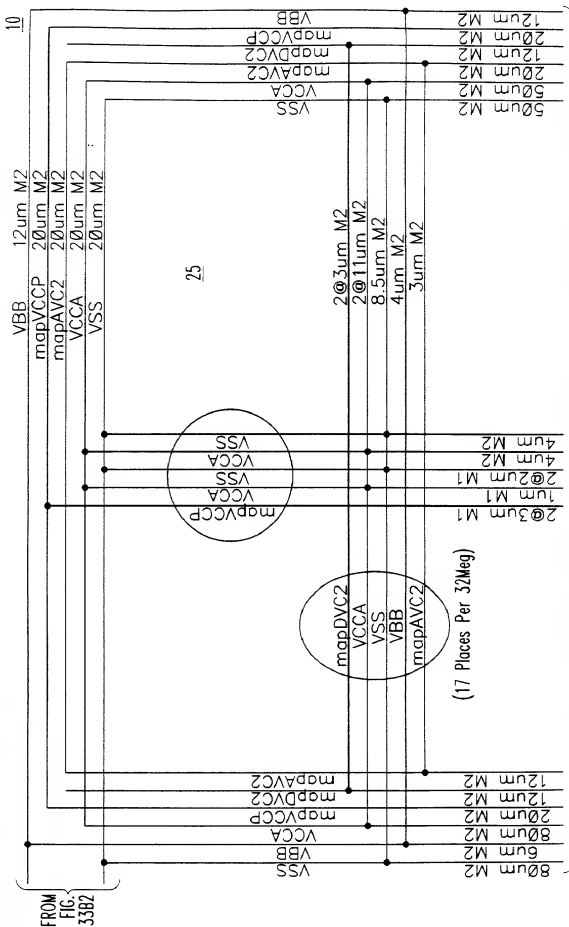


FIG. 33B7

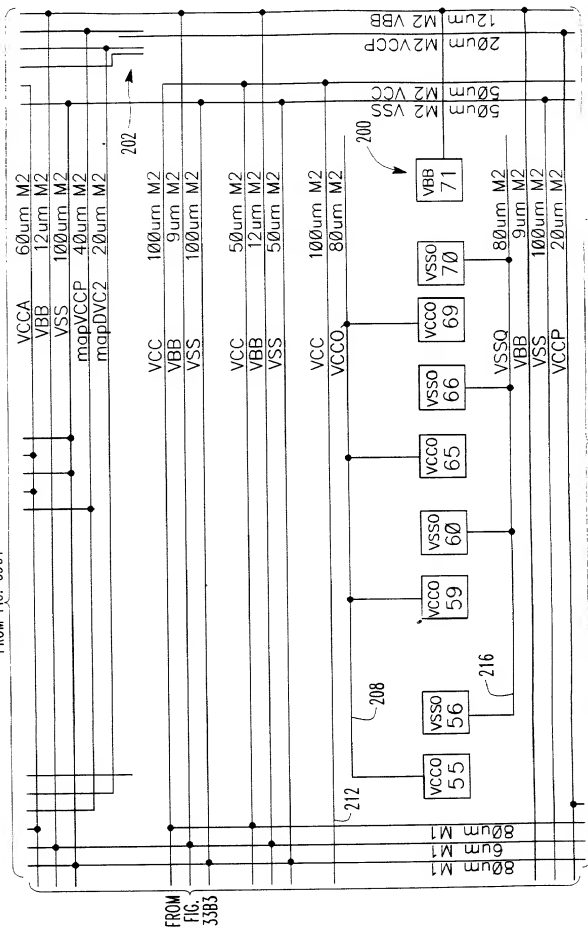




10 FIG. 33C2

FIG. 33C1

FROM FIG. 33C1



TO FIG. 33C3

FIG. 33C2

FROM FIG. 33C2

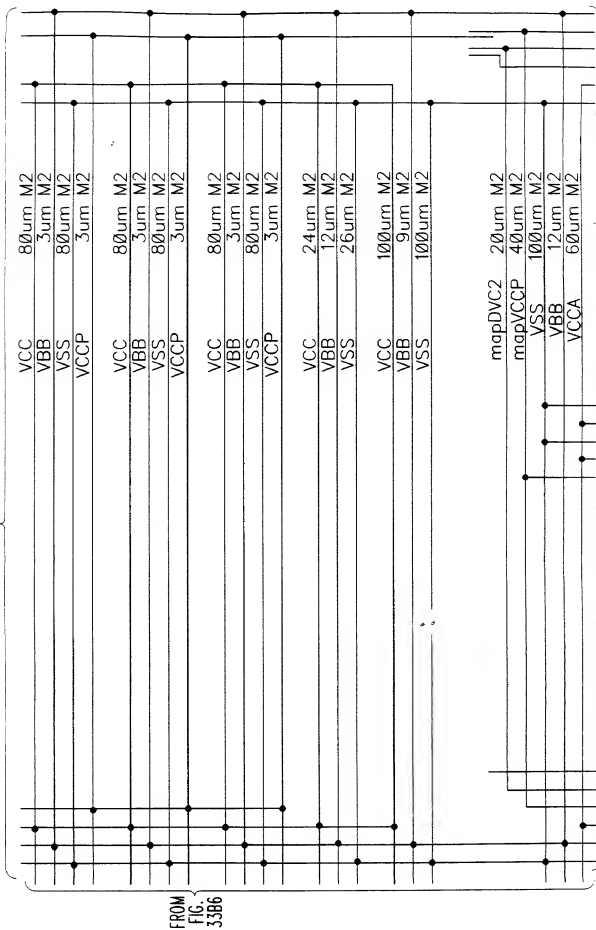
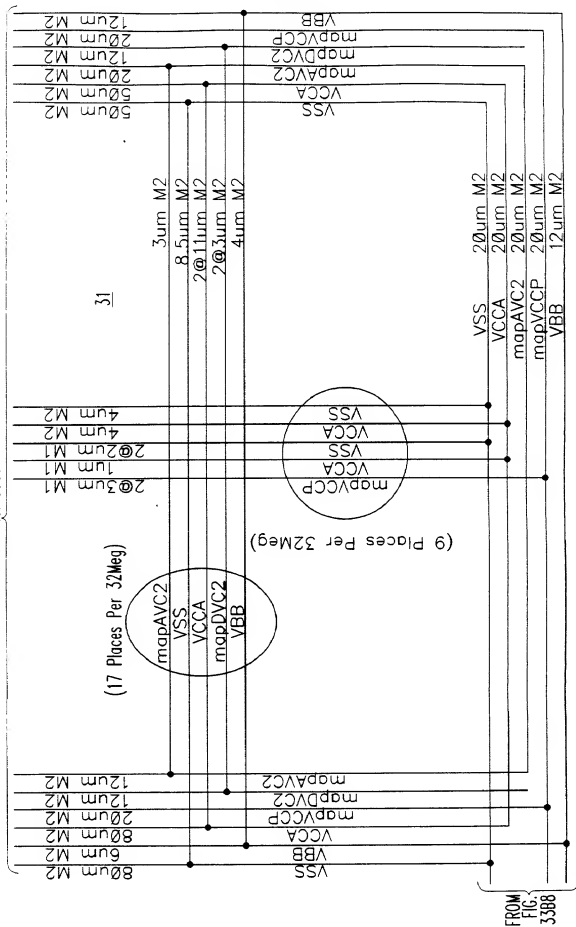


FIG. 33C3

FROM FIG. 33C3



FROM
FIG.
33B8

FIG. 33C4

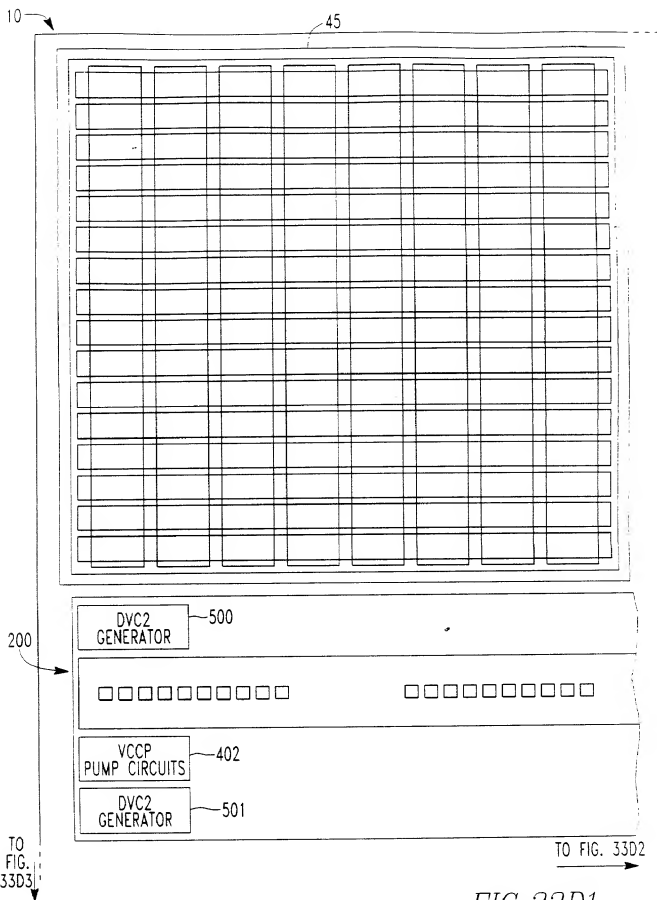


FIG. 33D1

TO FIG. 33D1

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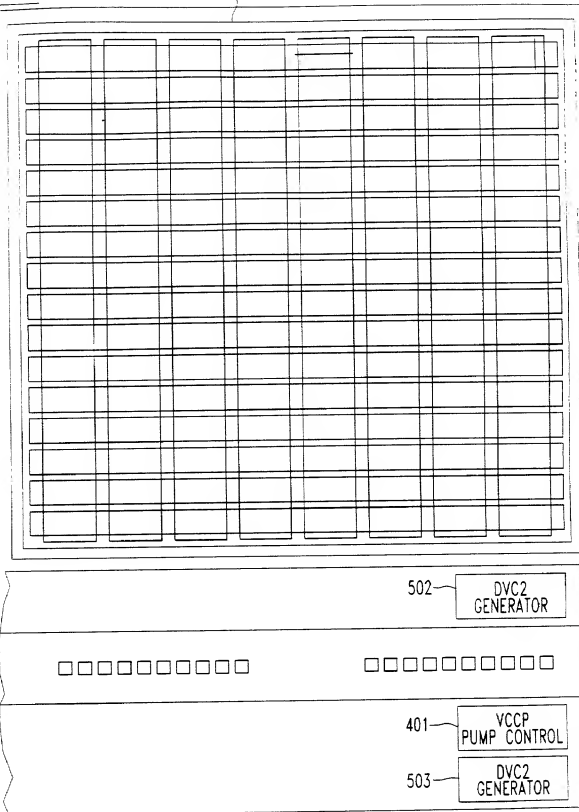
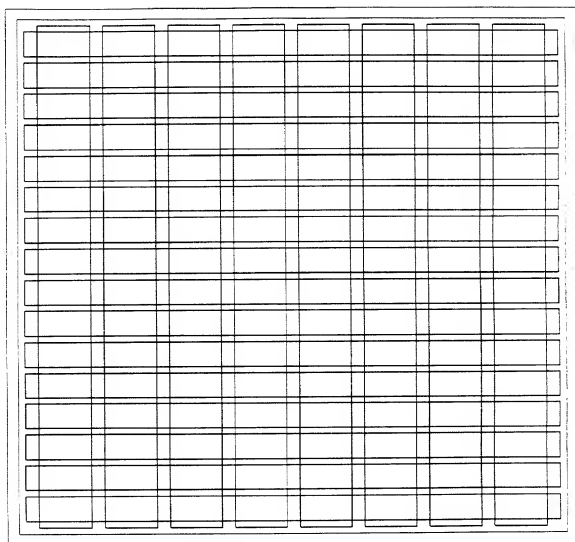
TO
FIG.
33D4

FIG. 33D2

TO
FIG.
33D1

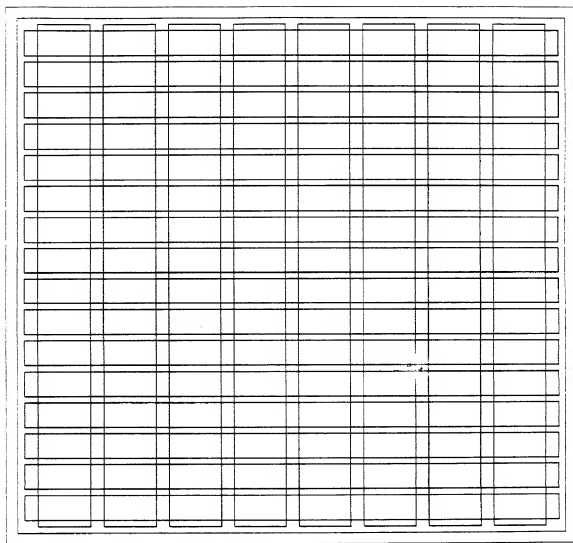
(SEE FIG. 33E1)



TO FIG. 33D4

FIG. 33D3

TO
FIG.
33D2



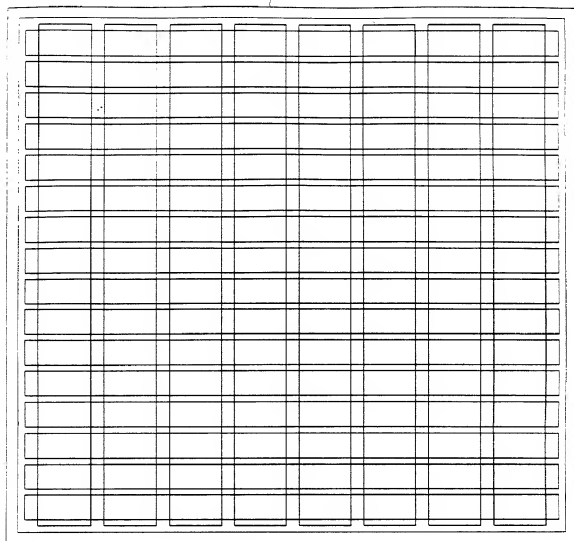
TO FIG. 33D3

FIG. 33D4

(SEE FIG. 33D2)

25

TO FIG. 33E2



DVC2
GENERATOR 504

□ □ □ □ □ □ □ □

□ □ □ □ □ □ □ □

VCCP
REGULATOR 220

DVC2
GENERATOR 505

TO
FIG.
33E3

FIG. 33E1

TO FIG. 33E1

27

10

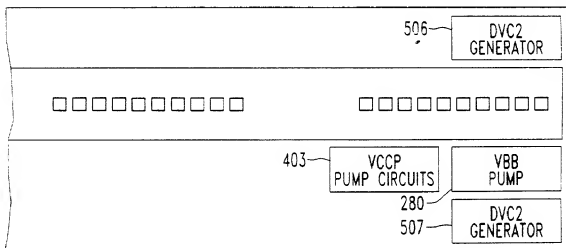
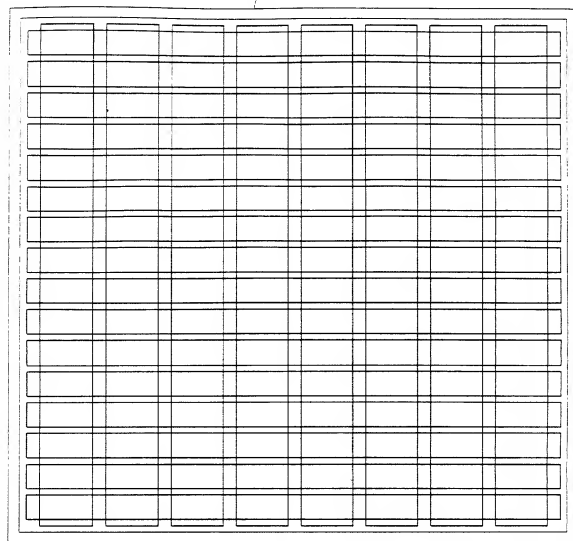
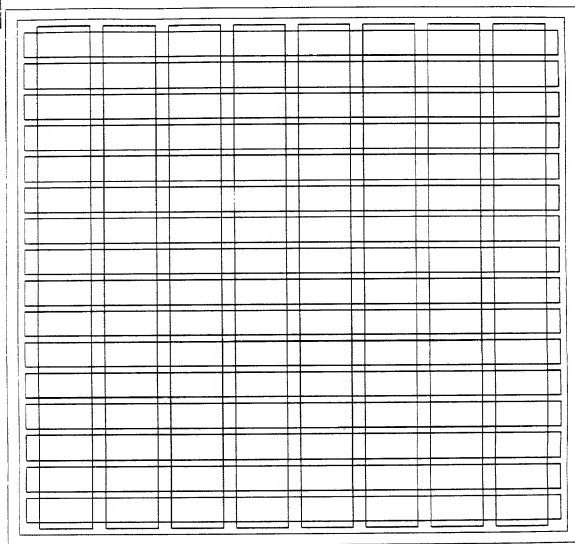


FIG. 33E2

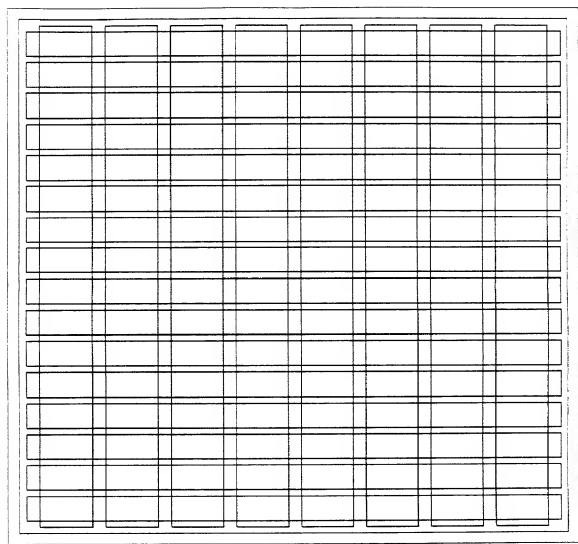
TO
FIG.
33E4

TO
FIG.
33E1

31

TO FIG. 33E4

FIG. 33E3



TO FIG. 33E3

FIG. 33E4

TO
FIG.
33E2

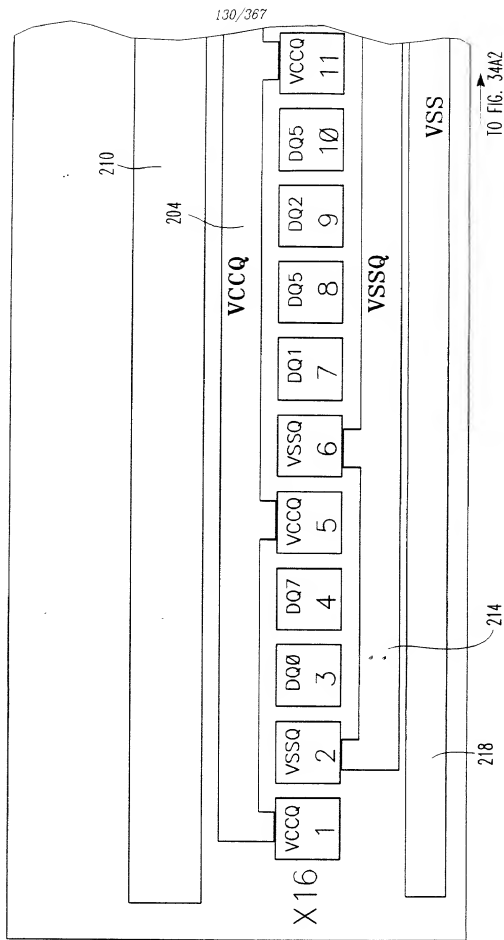
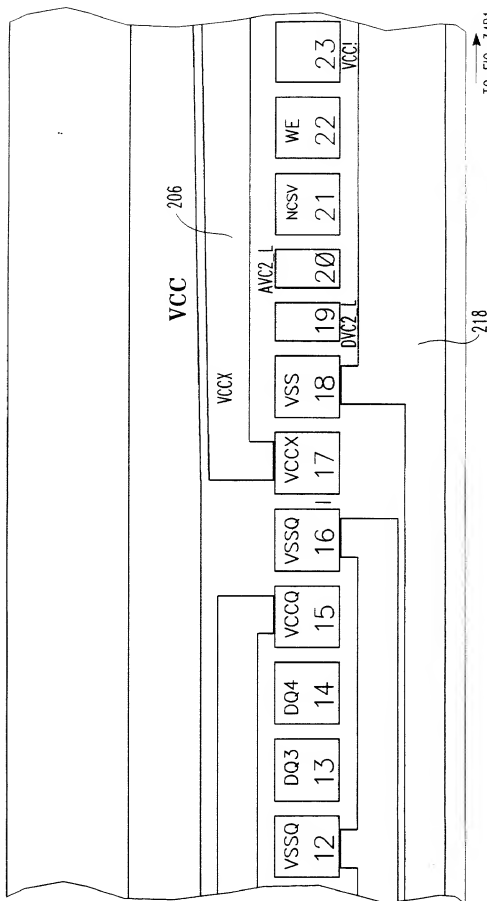


FIG. 34A1

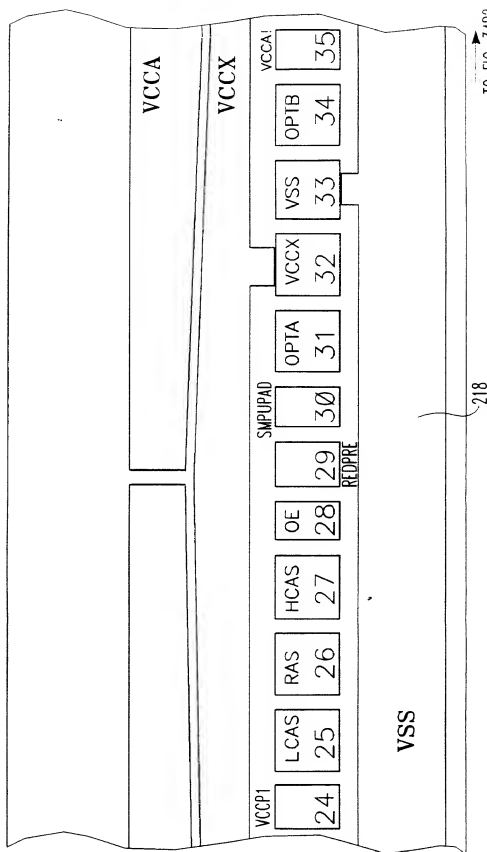
TO FIG. 34A1
←



TO FIG. 34B1
→

FIG. 34A2

TO FIG. 34A2



TO FIG. 34B2

FIG. 34B1

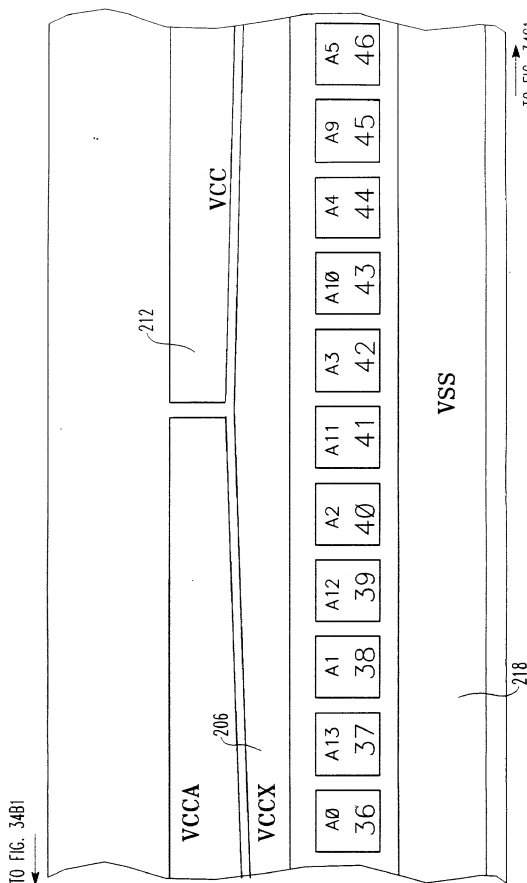
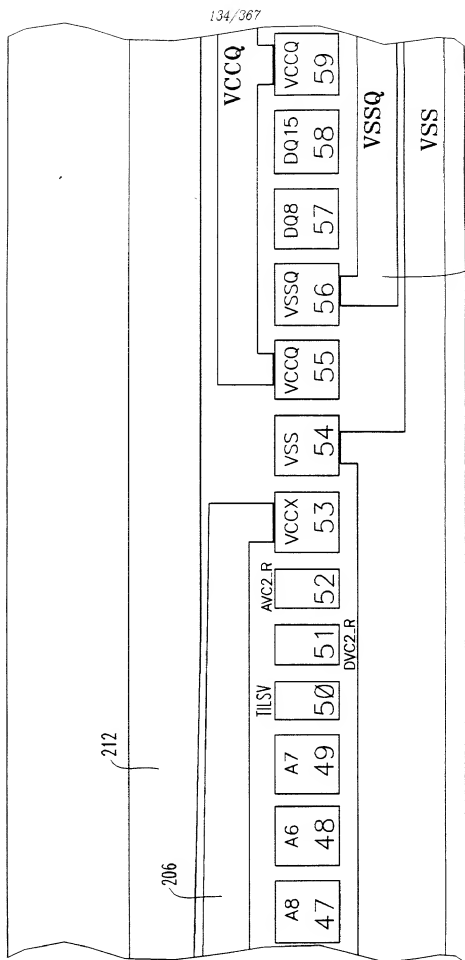


FIG. 3A

TO FIG. 34B2



TO FIG. 34C2

FIG. 34C1

TO FIG. 34C1

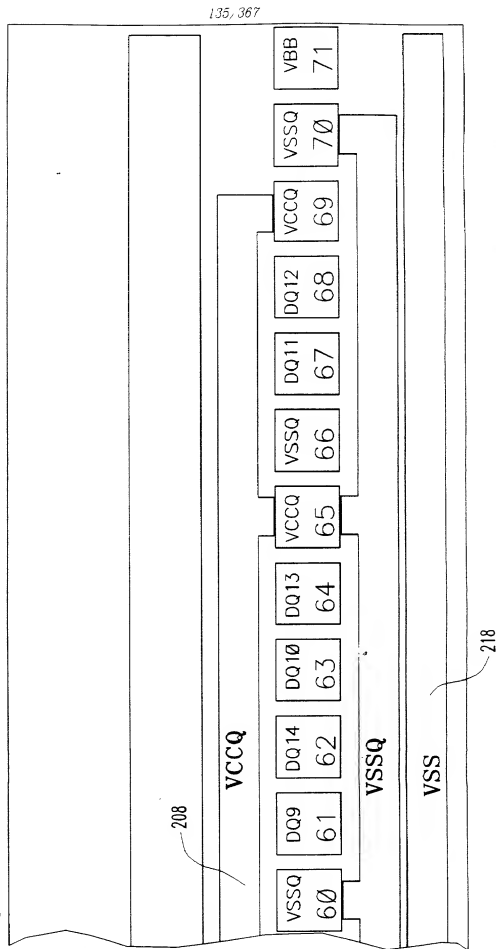


FIG. 34C2

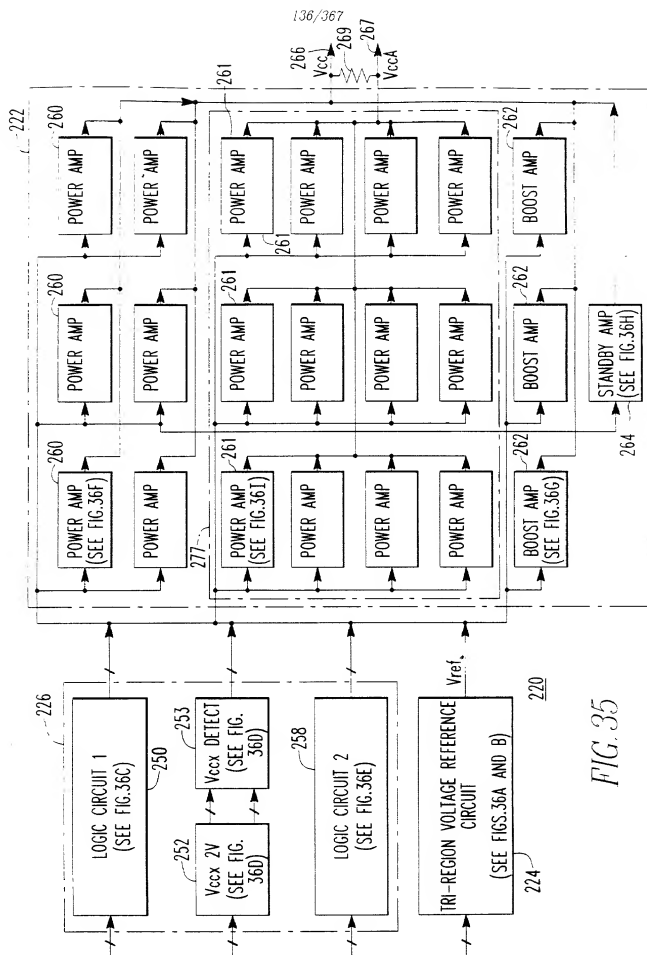


FIG. 35

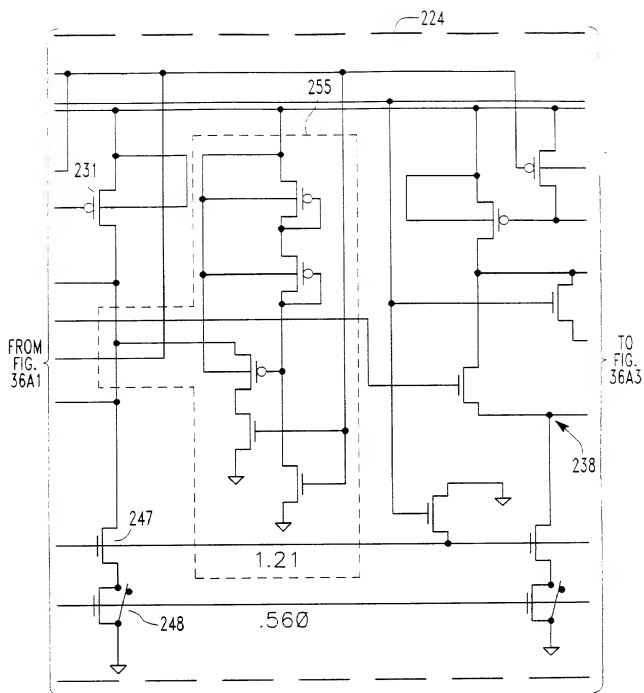


FIG. 36A2

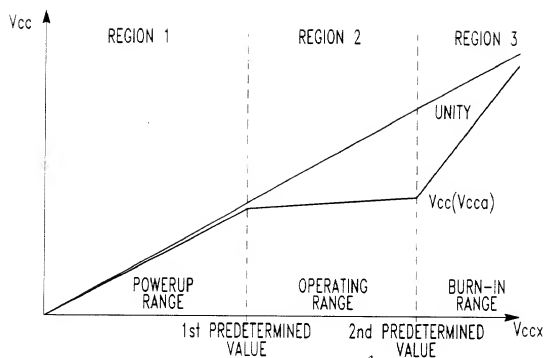


FIG. 36B

SEL32M<0:7>

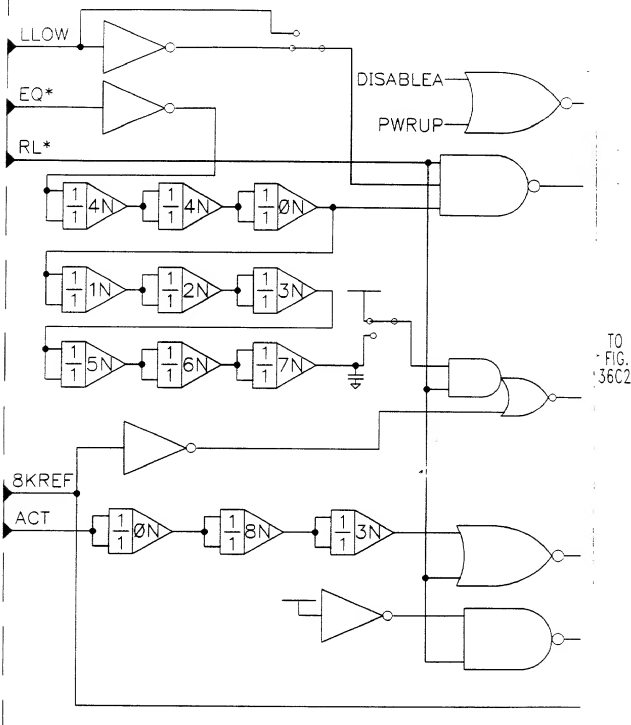
TO
FIG.
36C2

FIG. 36C1

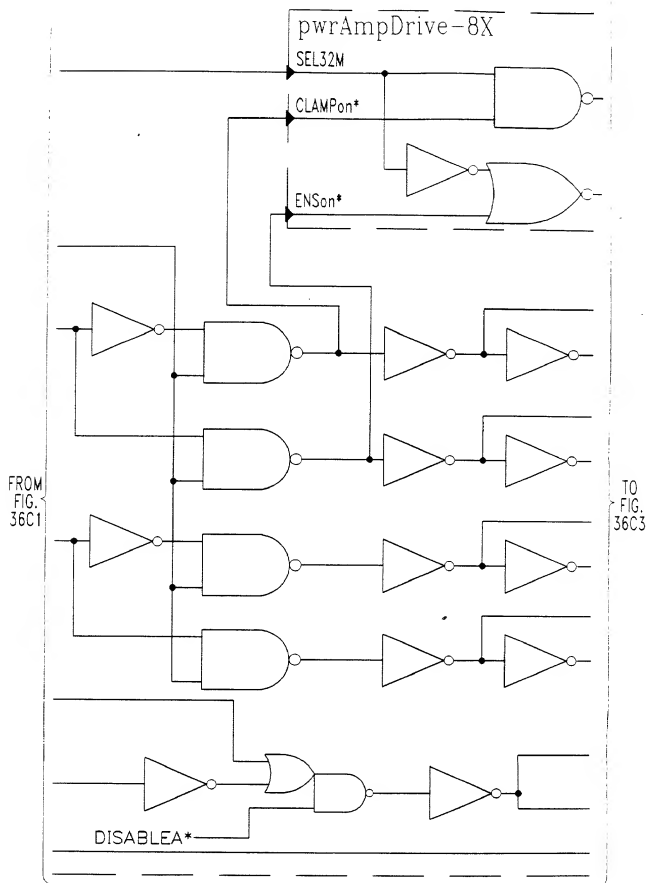


FIG. 36C2

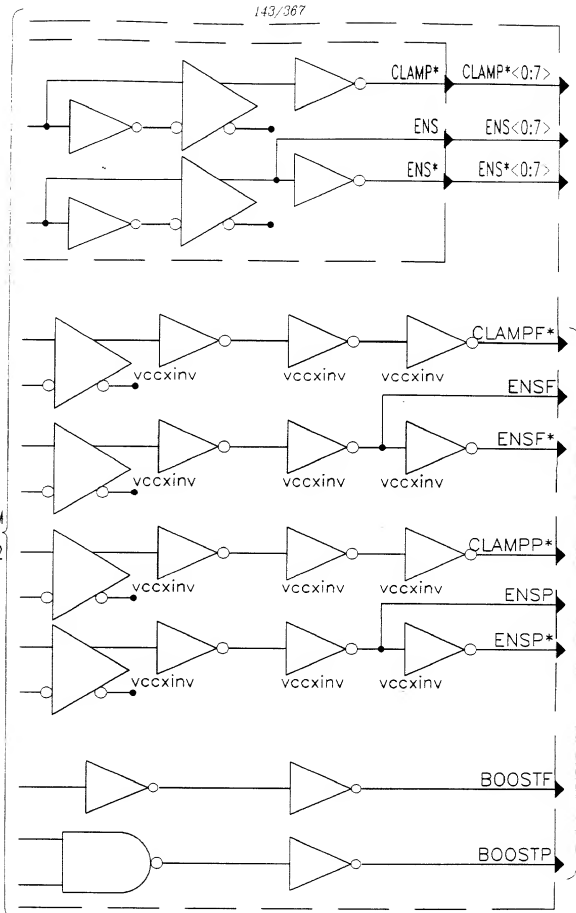
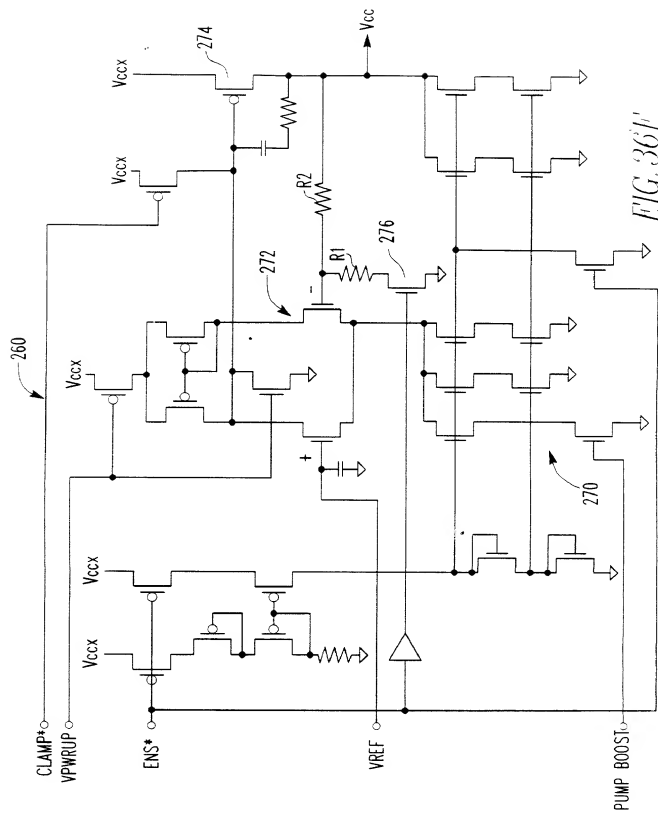
FROM
FIG.
36C2TO
FIG.
36F

FIG. 36C3



FIG. 36D



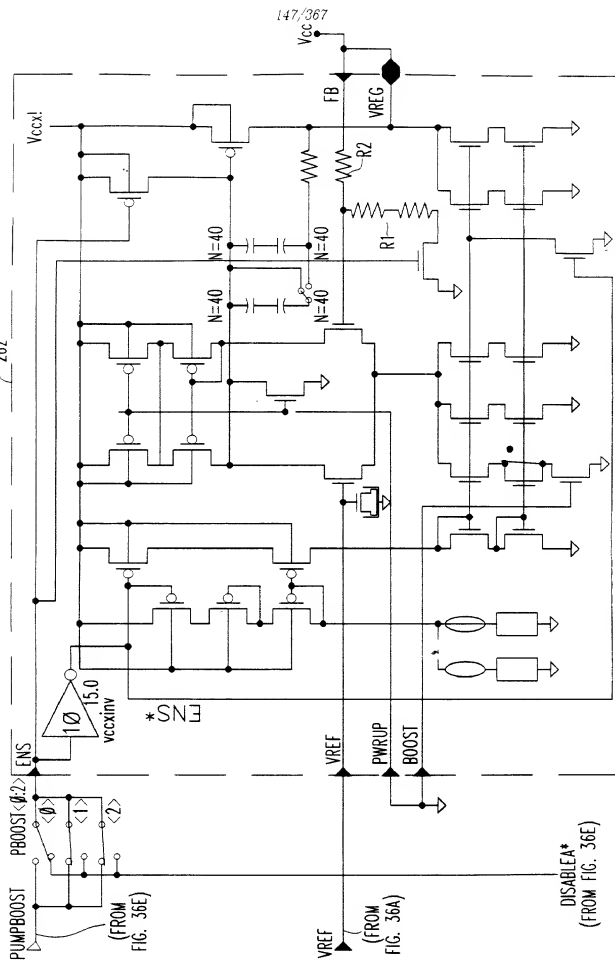
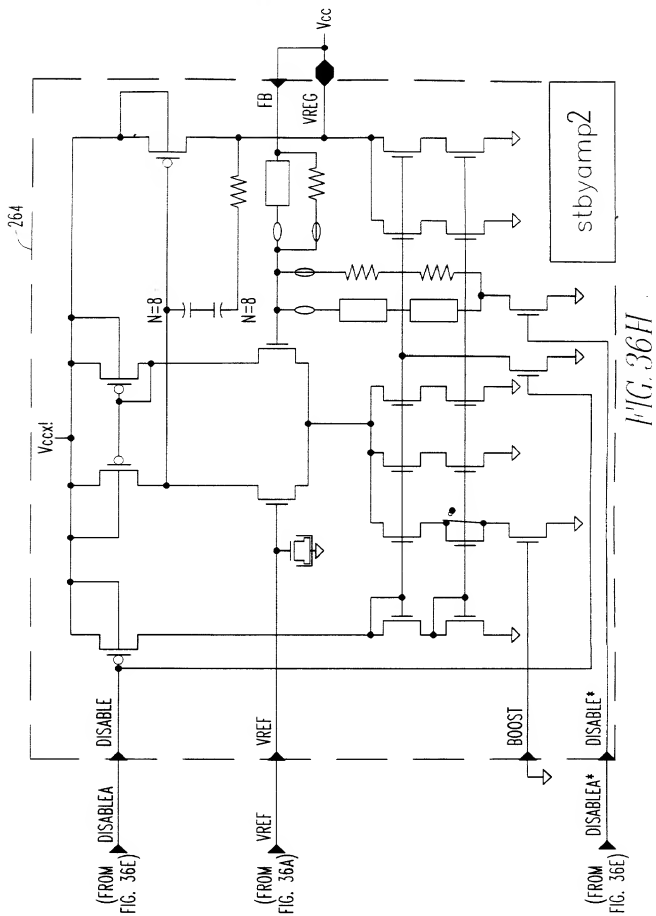


FIG. 36G



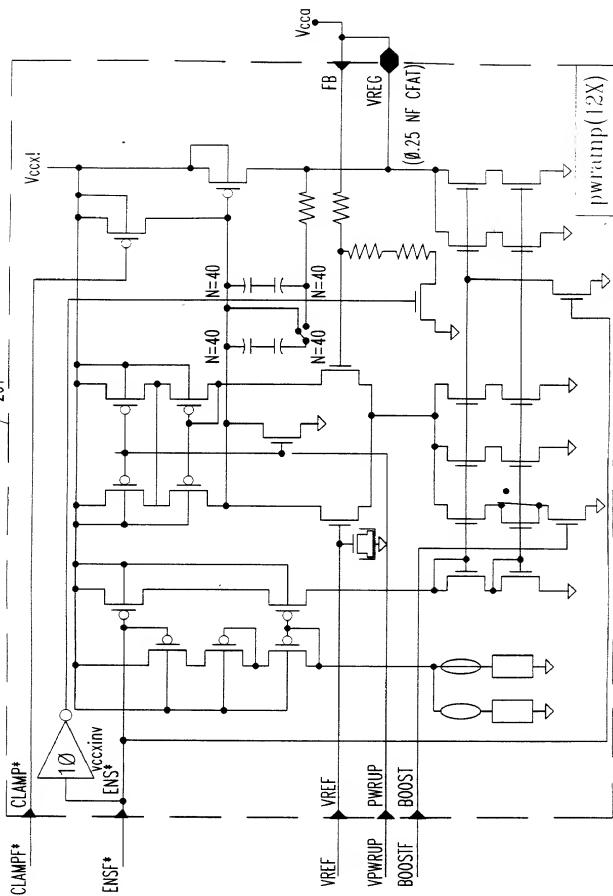


FIG. 361

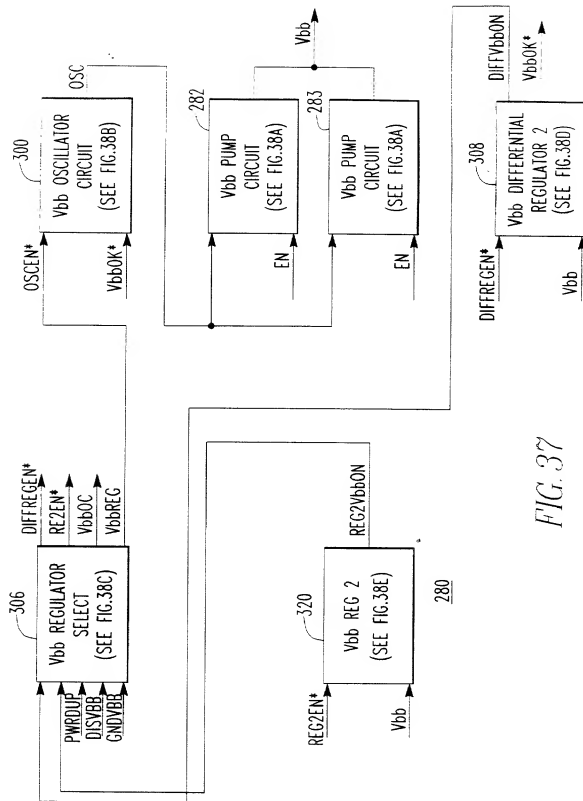


FIG. 37

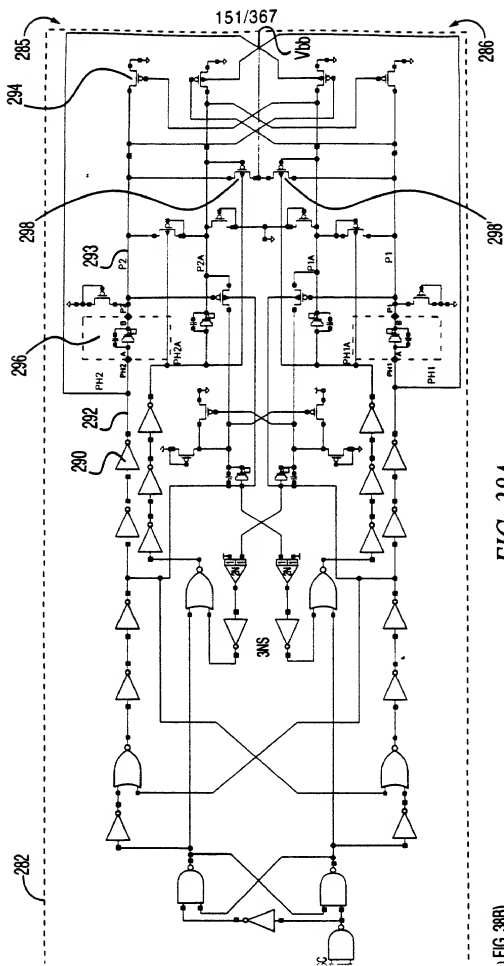


FIG. 38A

FIG. 38B

FIG. 38C) OSCEN*

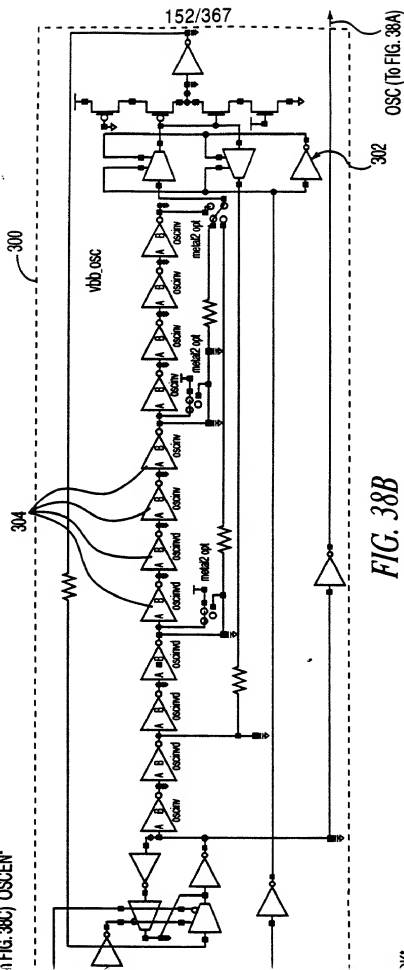
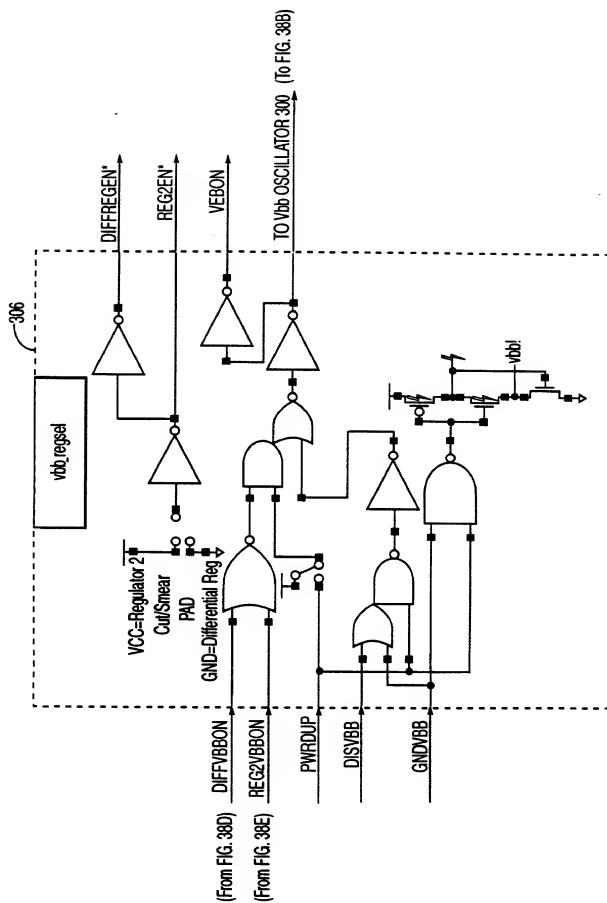


FIG. 38B



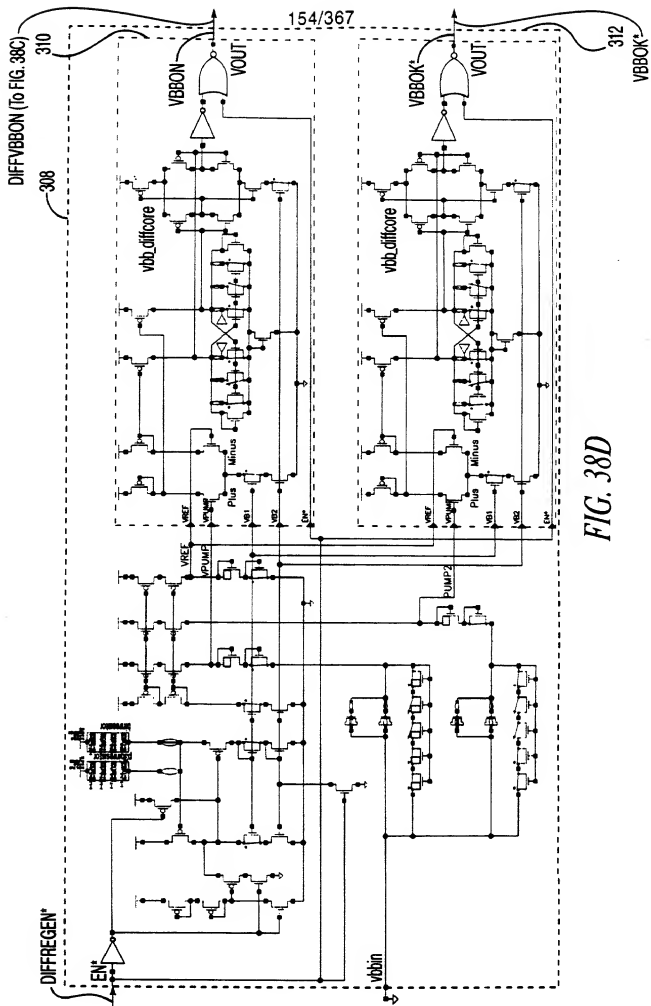


FIG. 38D

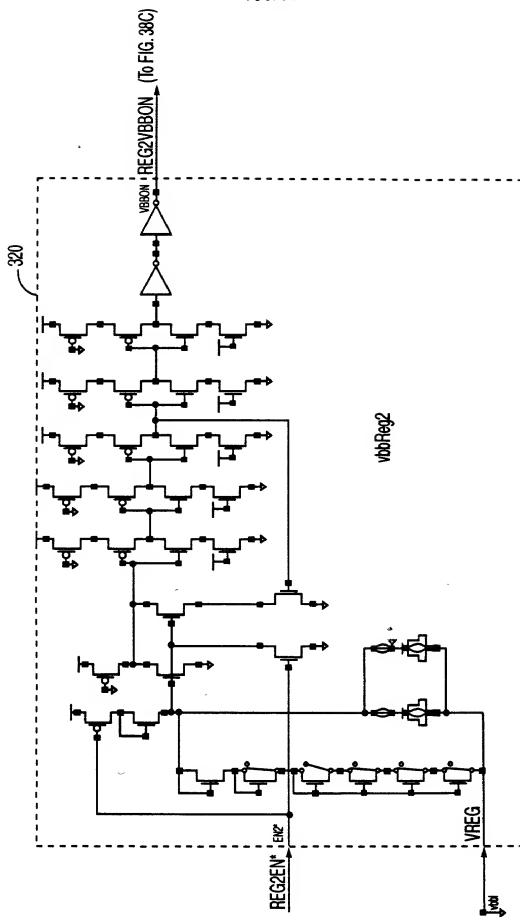
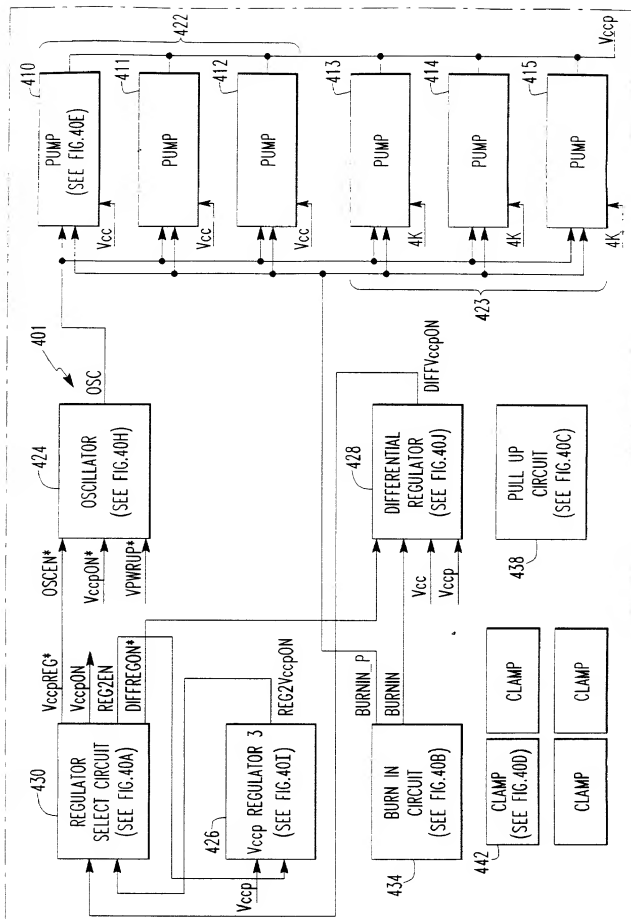


FIG. 38E



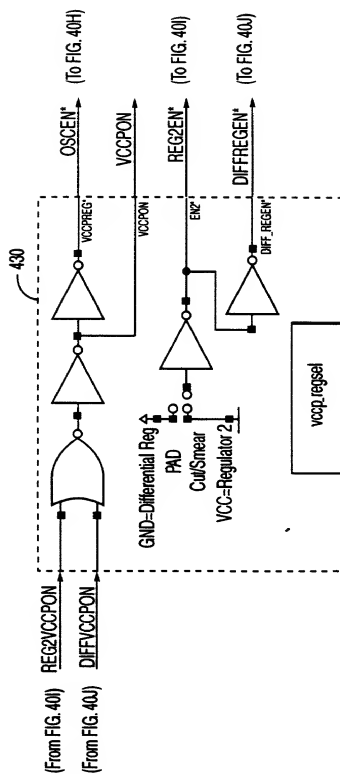


FIG. 40A

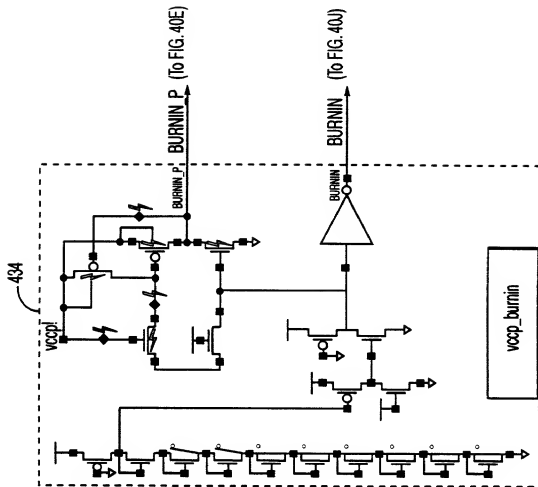


FIG. 40B

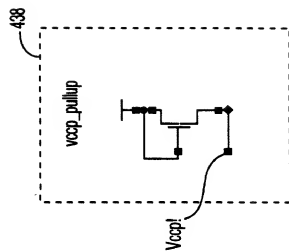


FIG. 40C

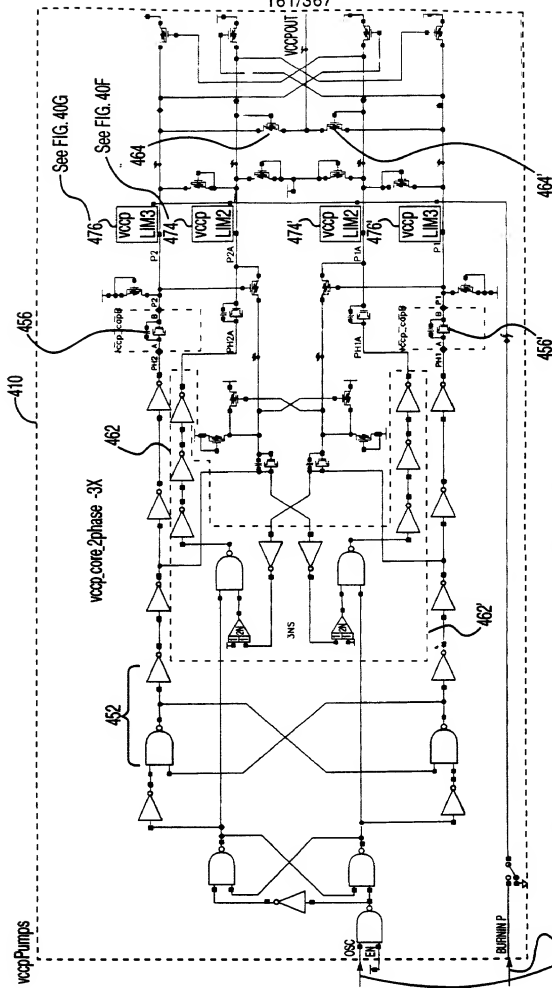


FIG. 40E

(From FIG. 40B) BURNNIN P

(From FIG. 40H) VCCPOSC

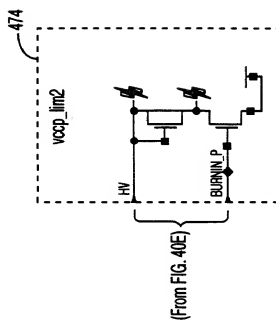


FIG. 40F

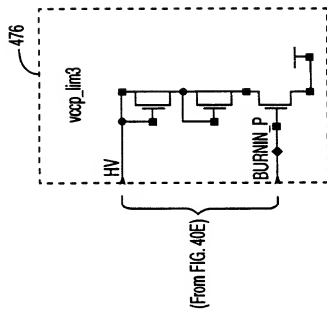


FIG. 40G

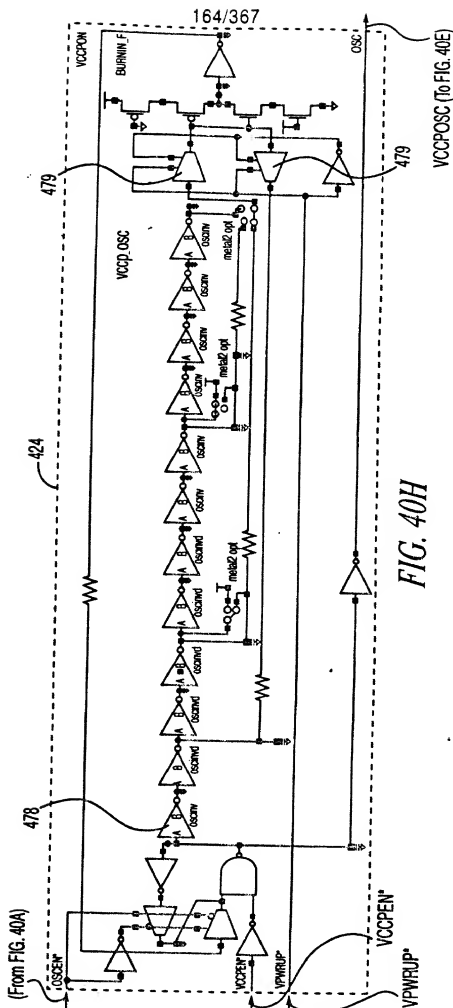


FIG. 40H

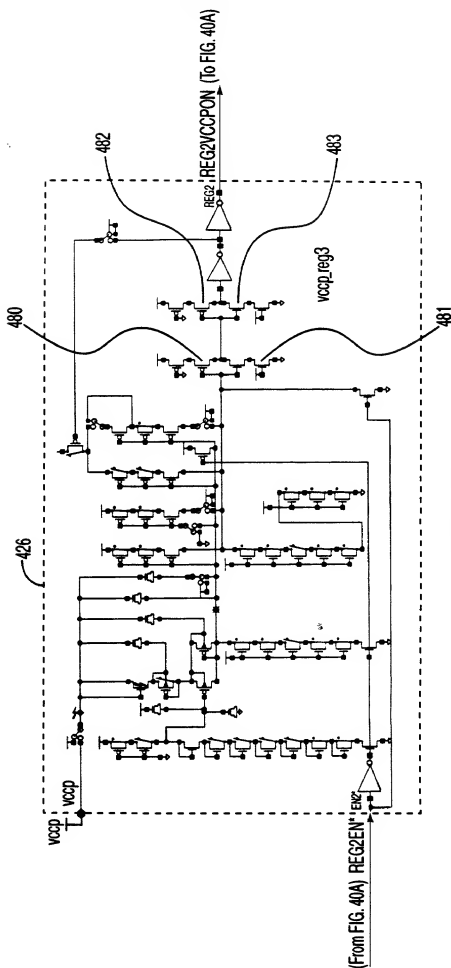


FIG. 401

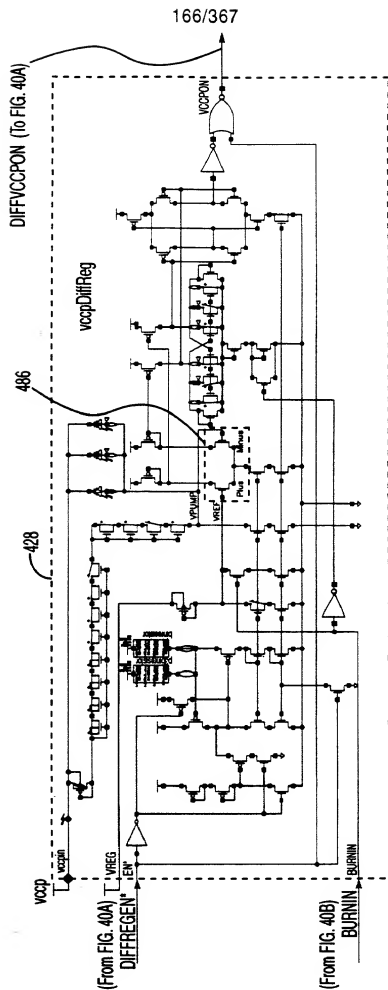


FIG. 40J

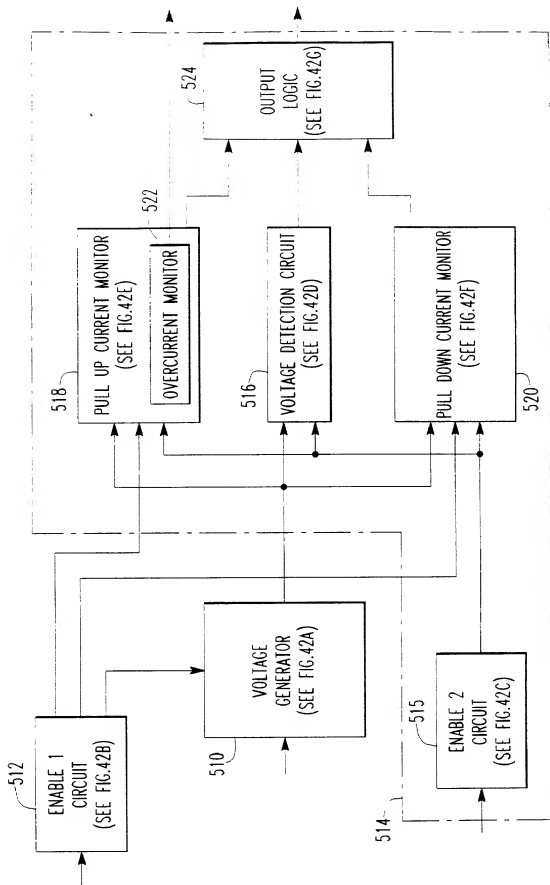


FIG. 1

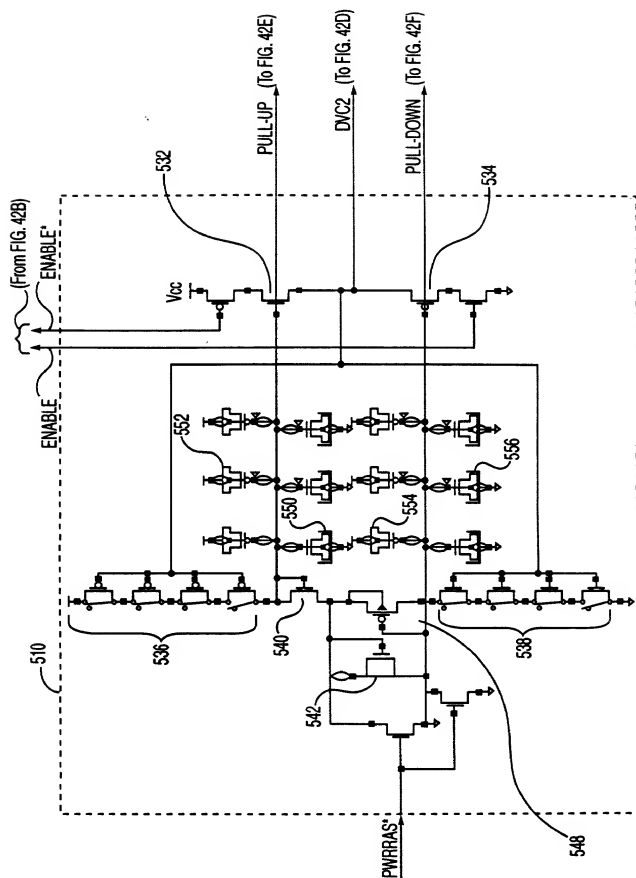


FIG. 42A

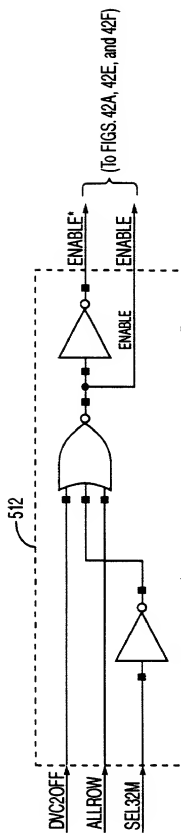


FIG. 42B

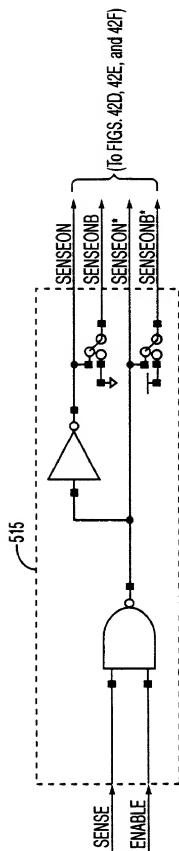


FIG. 42C

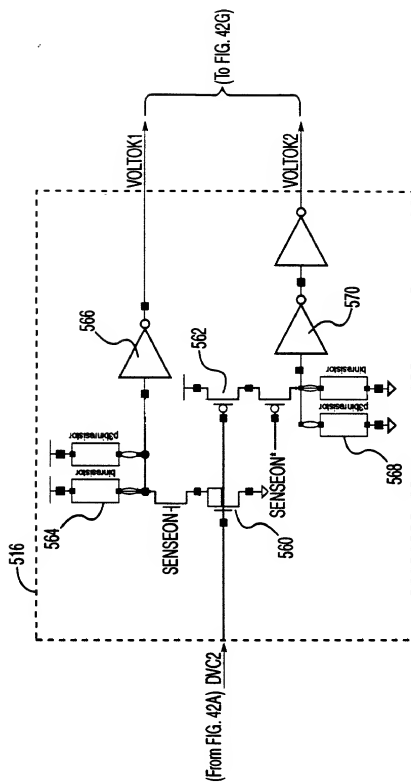


FIG. 42D

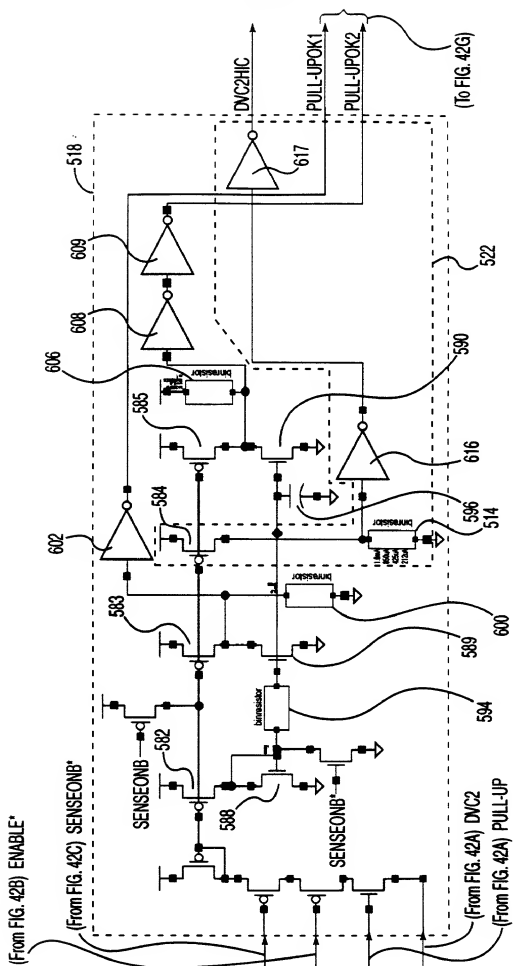


FIG. 42E

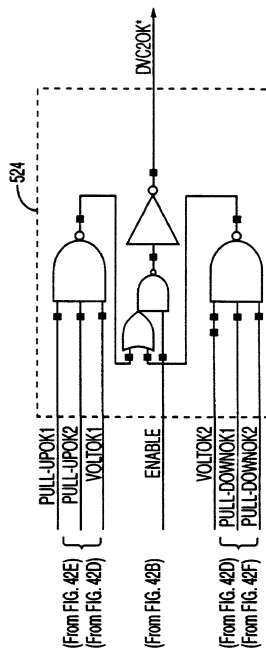


FIG. 42G

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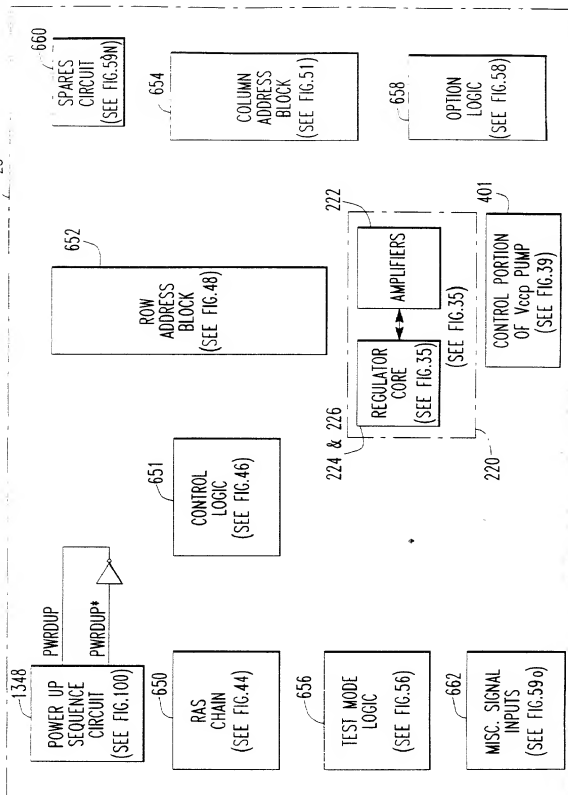
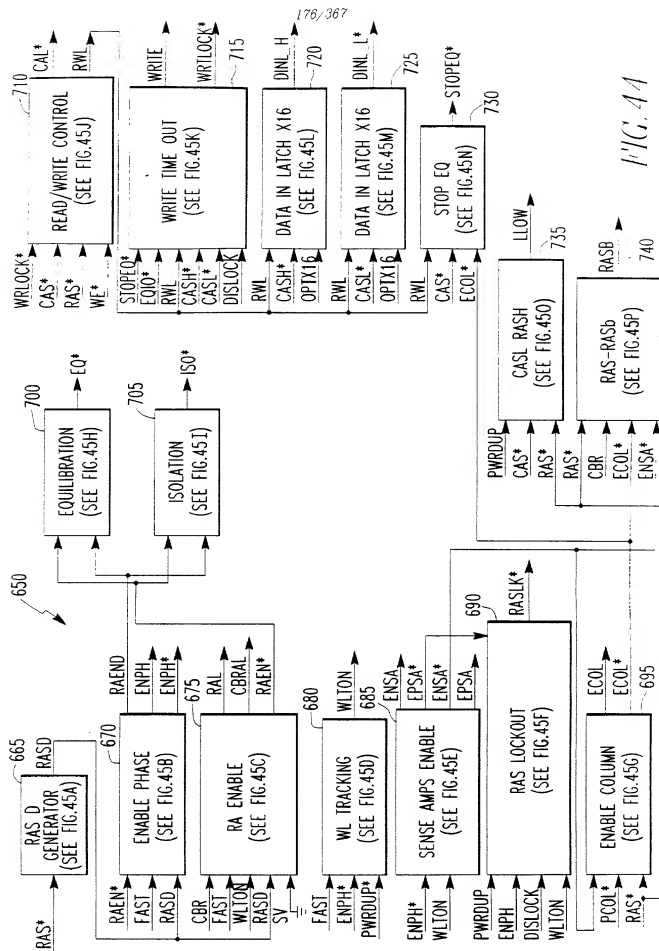


FIG. 4



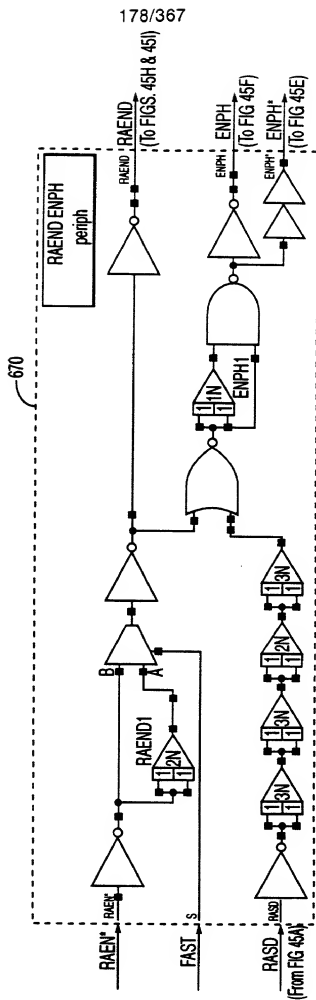


FIG. 45B

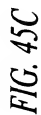


FIG. 45C

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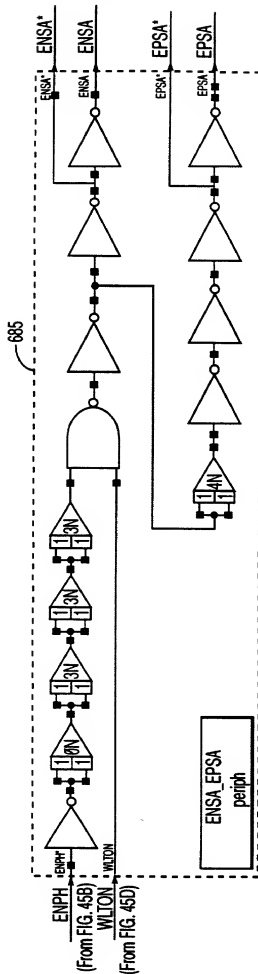


FIG. 45E

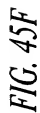


FIG. 45F

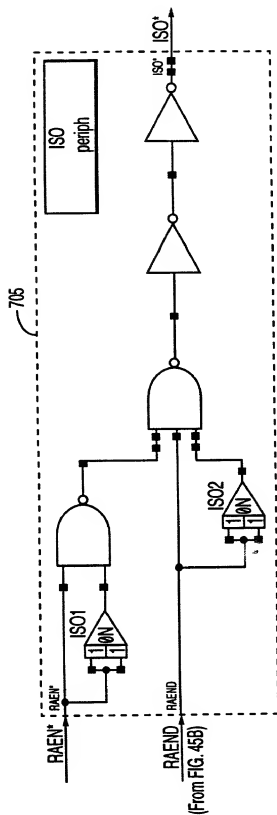


FIG. 45I



FIG. 45J

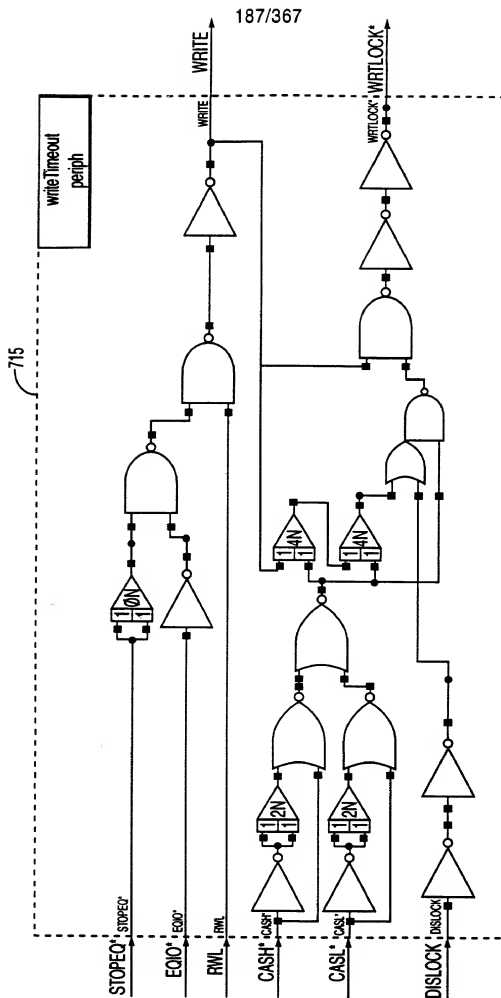


FIG. 45K

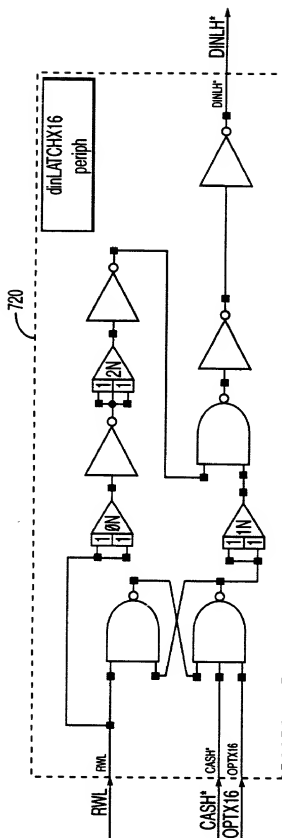


FIG. 45L

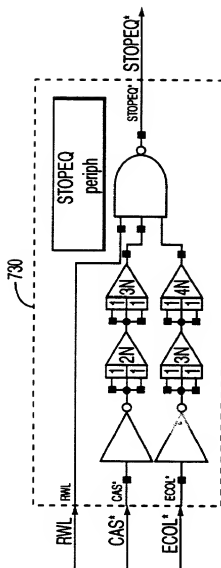


FIG. 45N

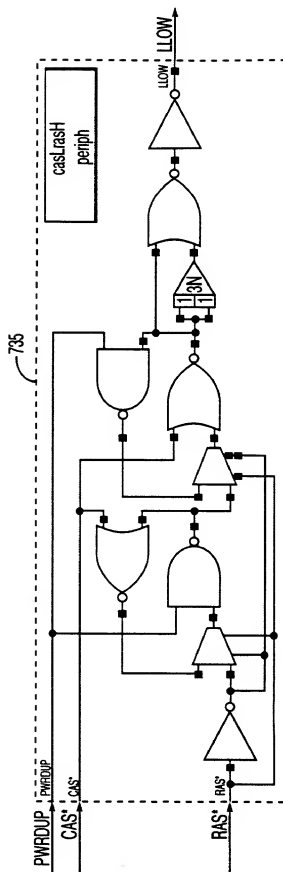


FIG. 450

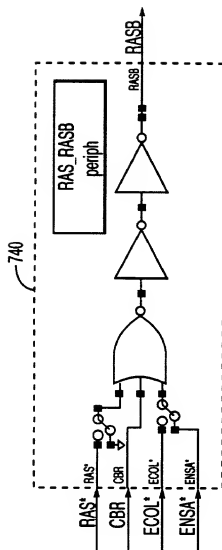


FIG. 45P



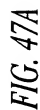


FIG. 47A

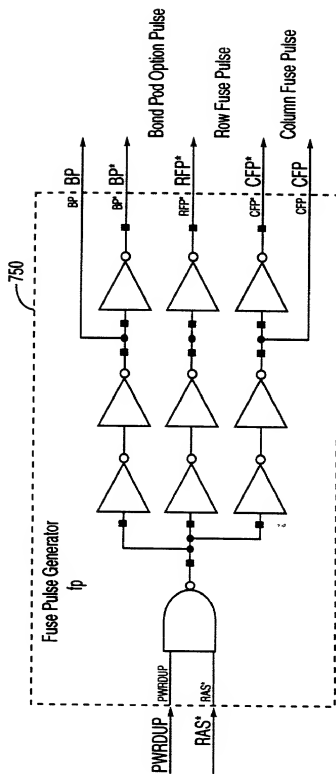


FIG. 47B

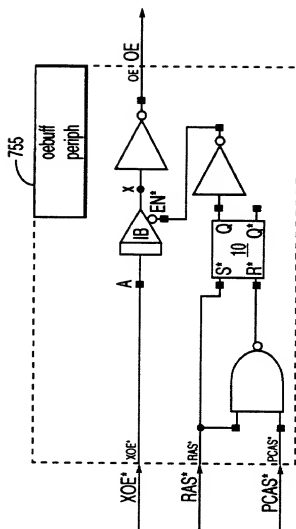


FIG. 47C

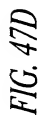


FIG. 47D

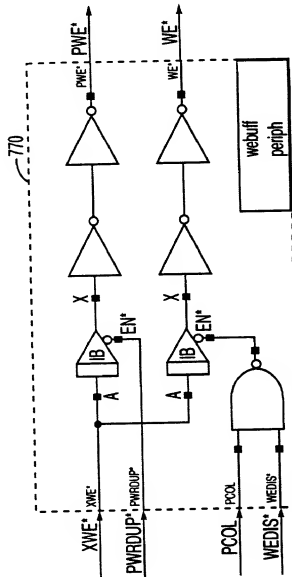


FIG. 47F

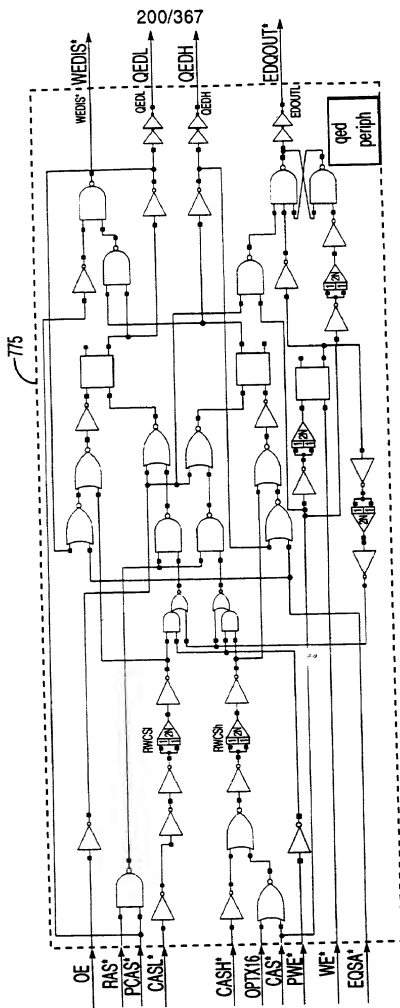
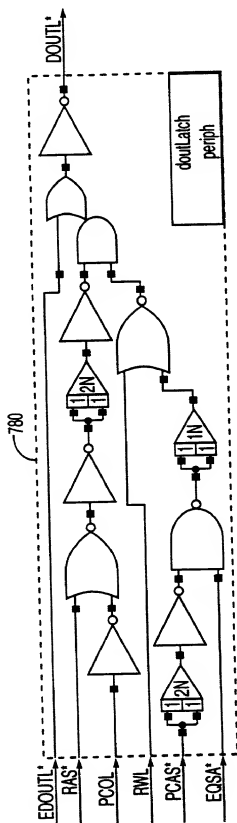


FIG. 47G



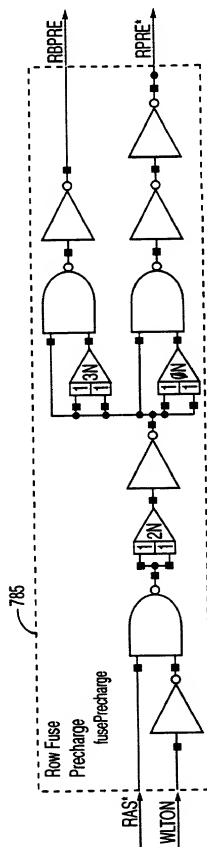


FIG. 471

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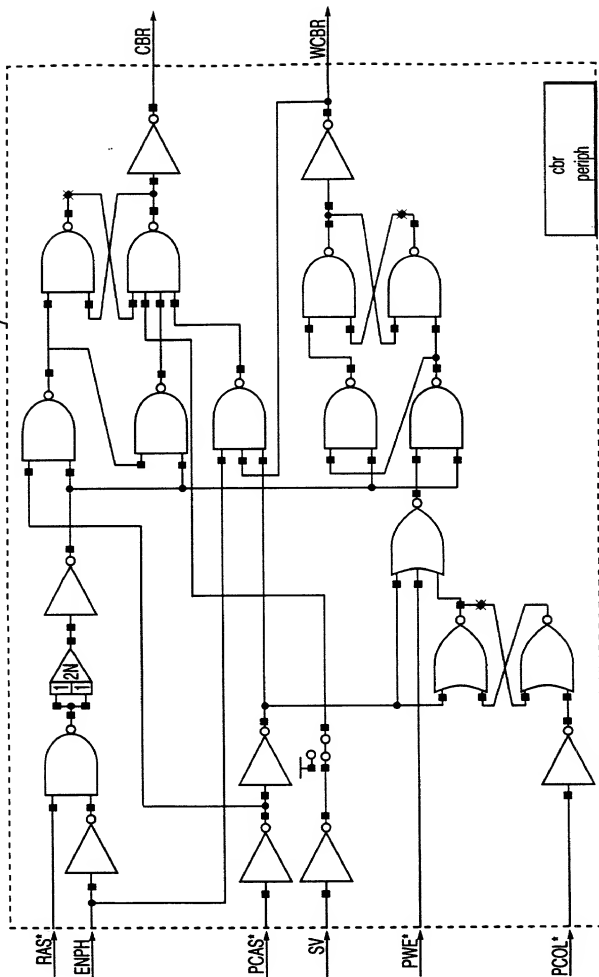


FIG. 47J

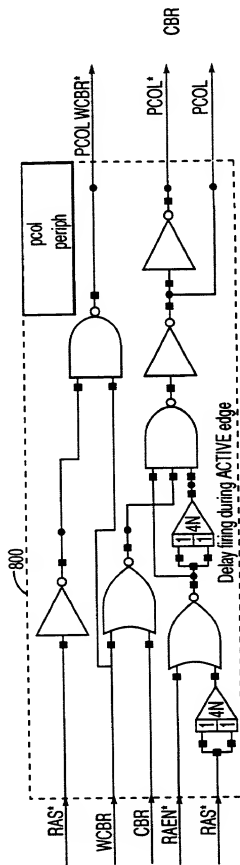


FIG. 47K

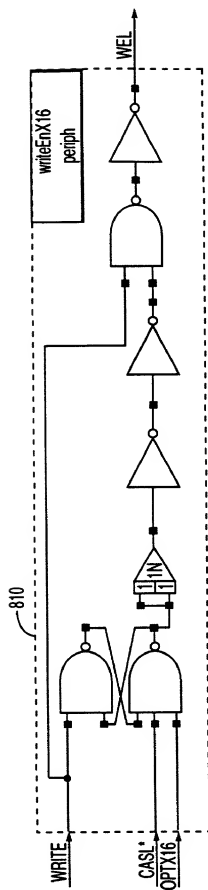


FIG. 47M

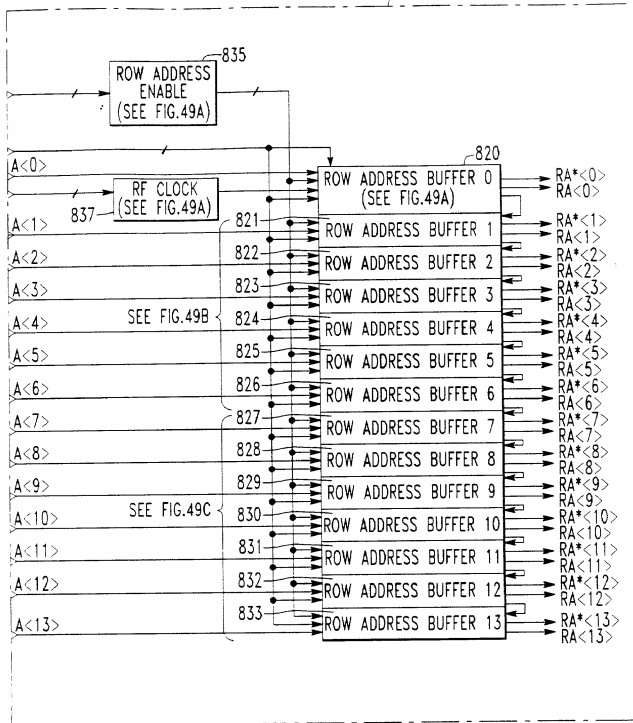


FIG. 48A

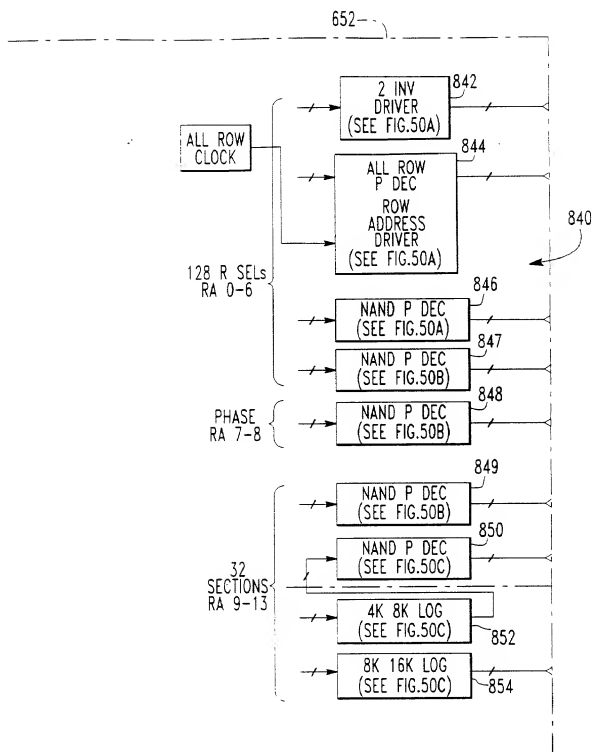


FIG. 48B

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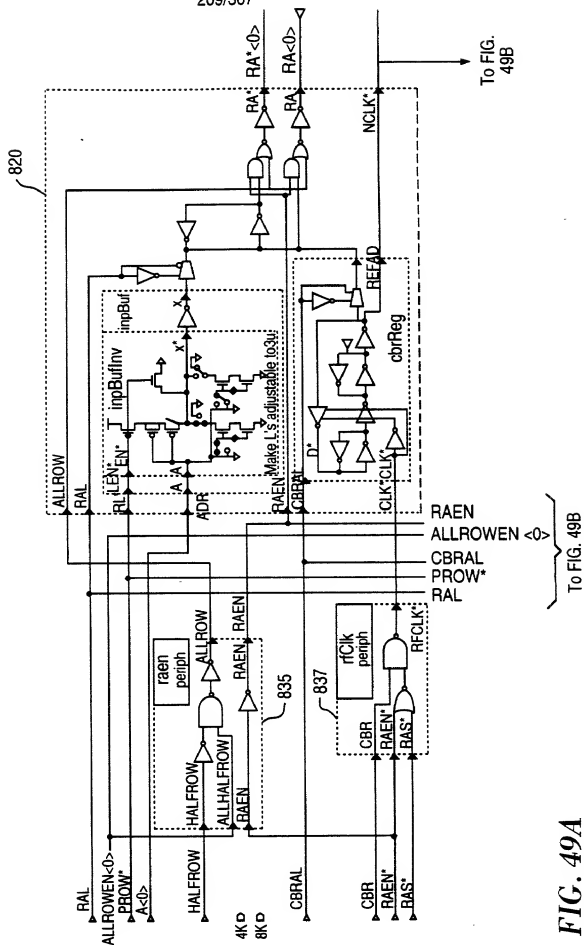
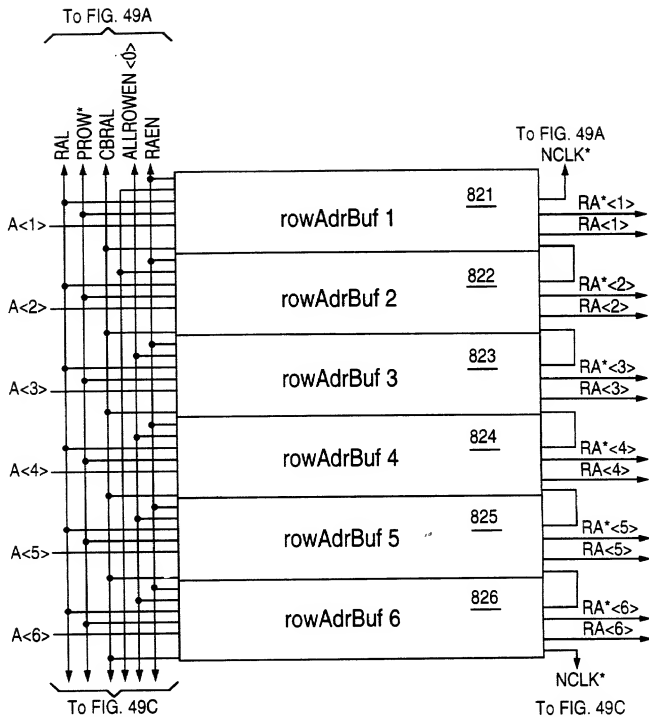
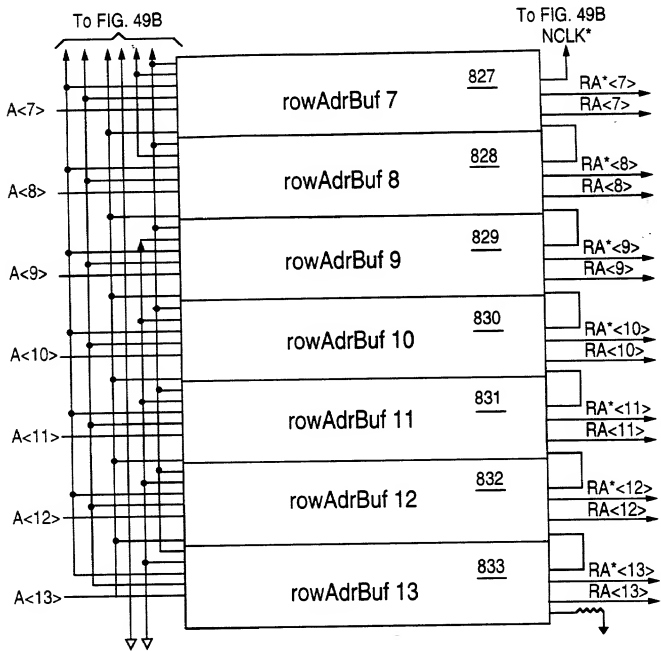


FIG. 49A

**FIG. 49B**

**FIG. 49C**

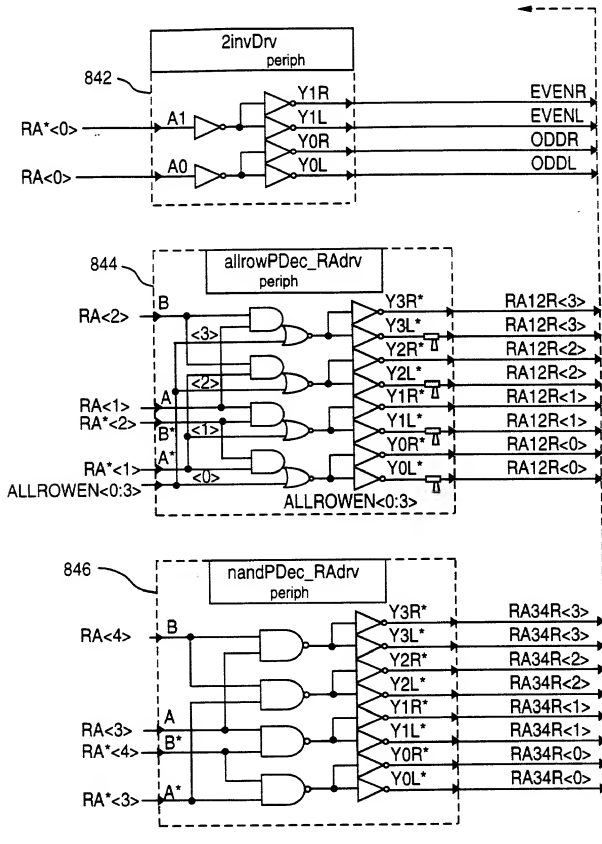
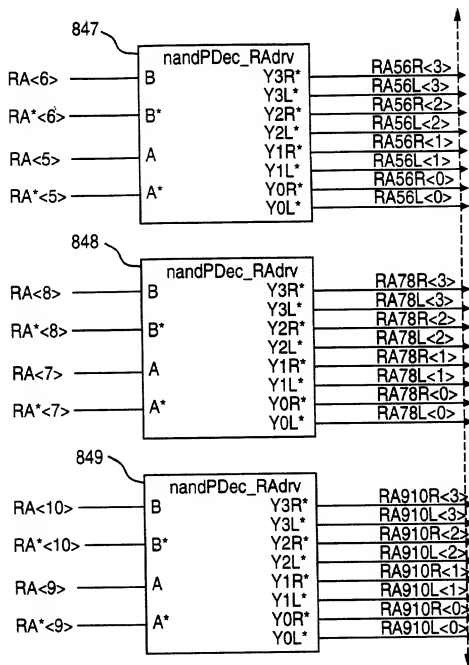


FIG. 50A

**FIG. 50B**

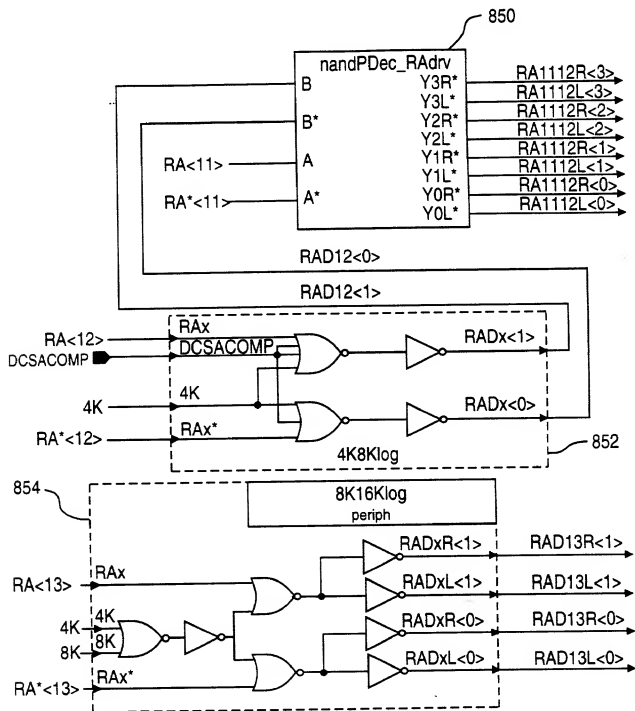


FIG. 50C

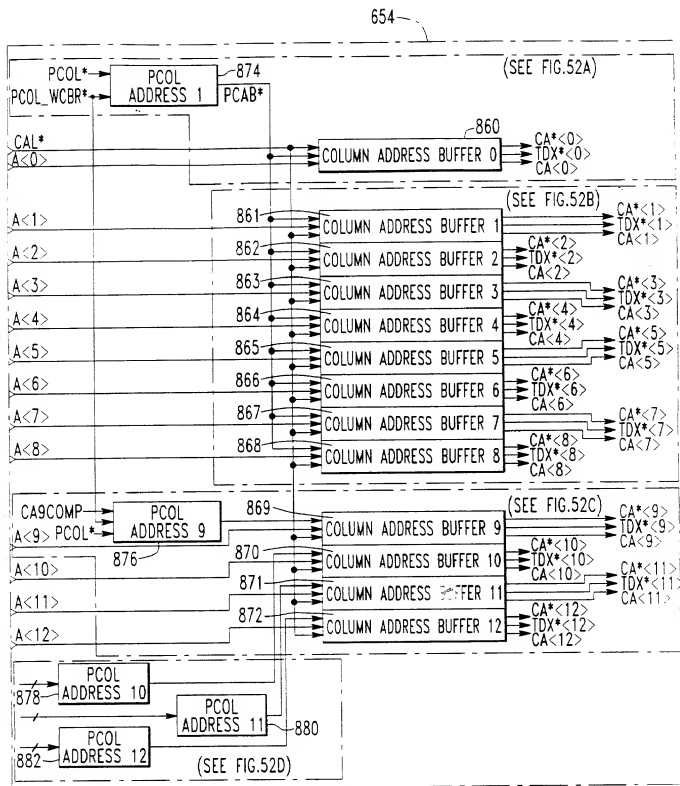


FIG. 51A

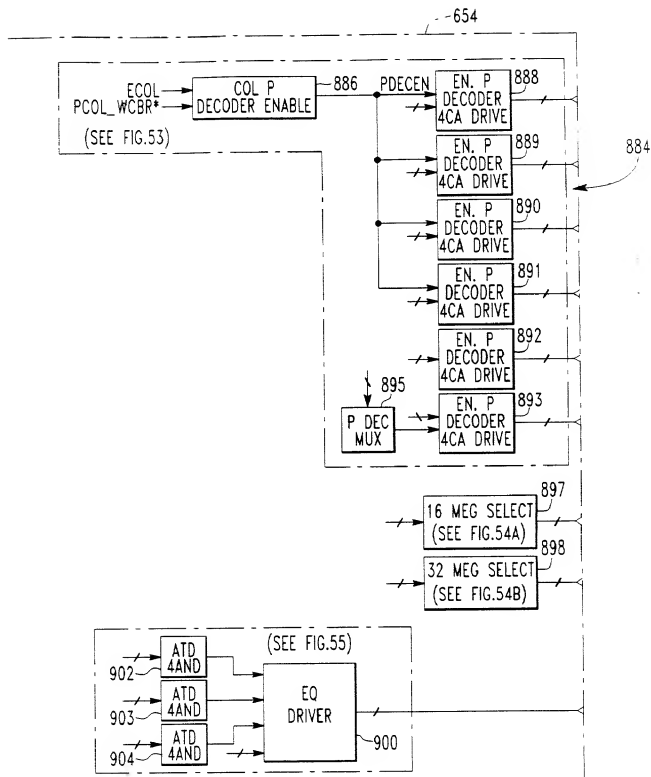


FIG. 51B

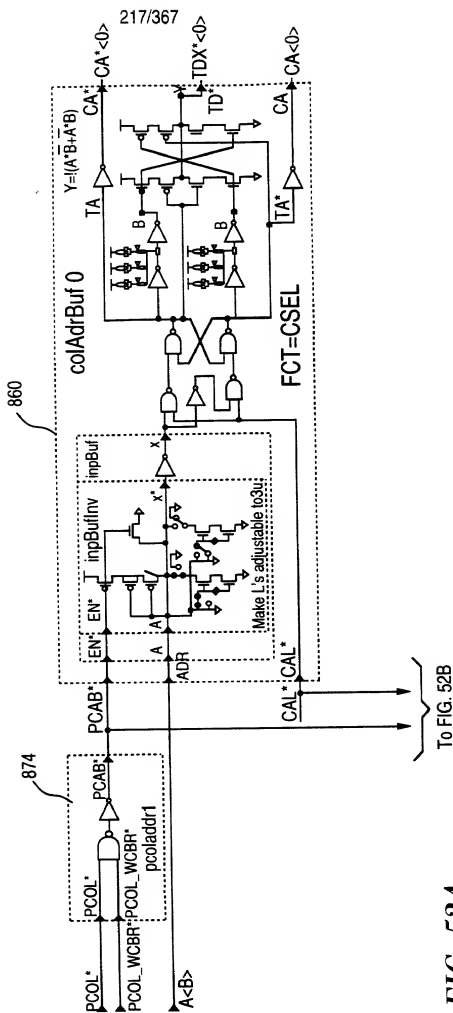


FIG. 52A

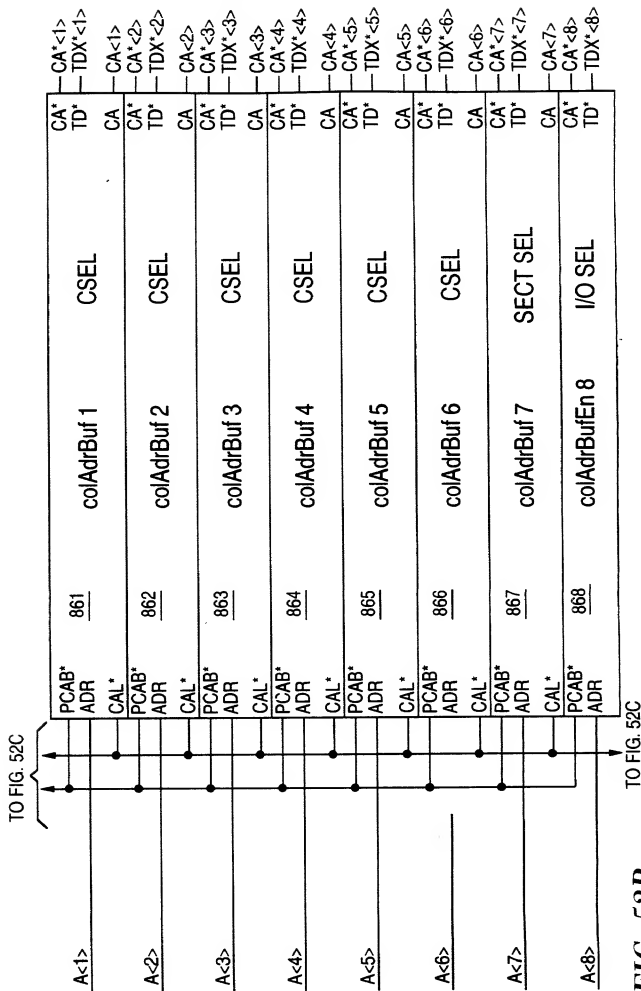


FIG. 52B

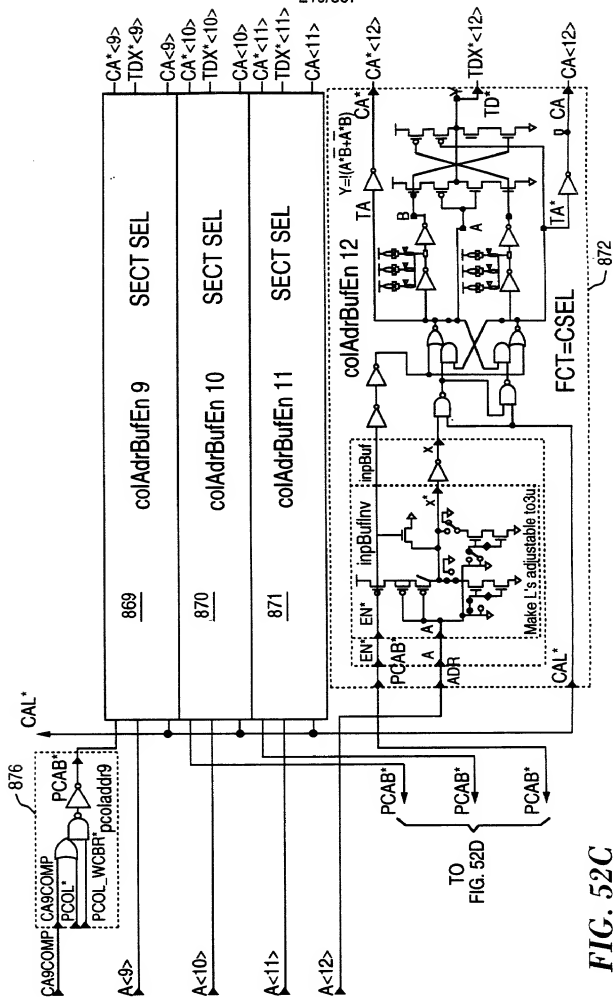


FIG. 52C

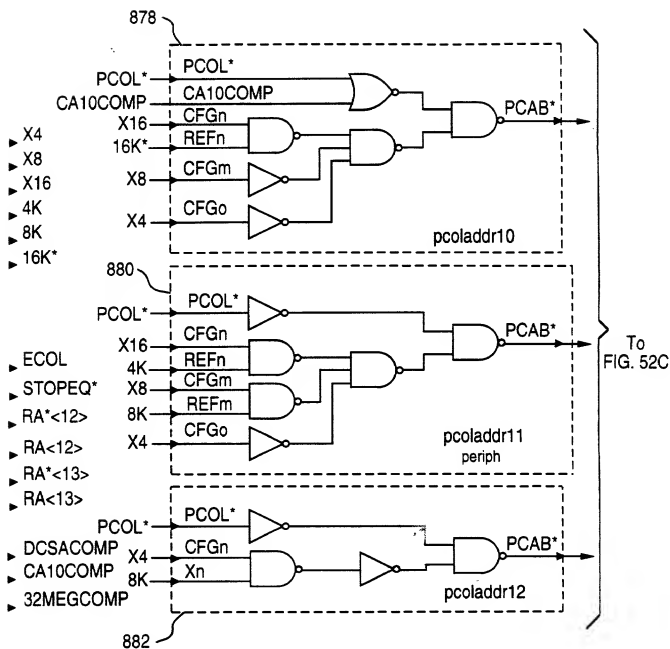


FIG. 52D

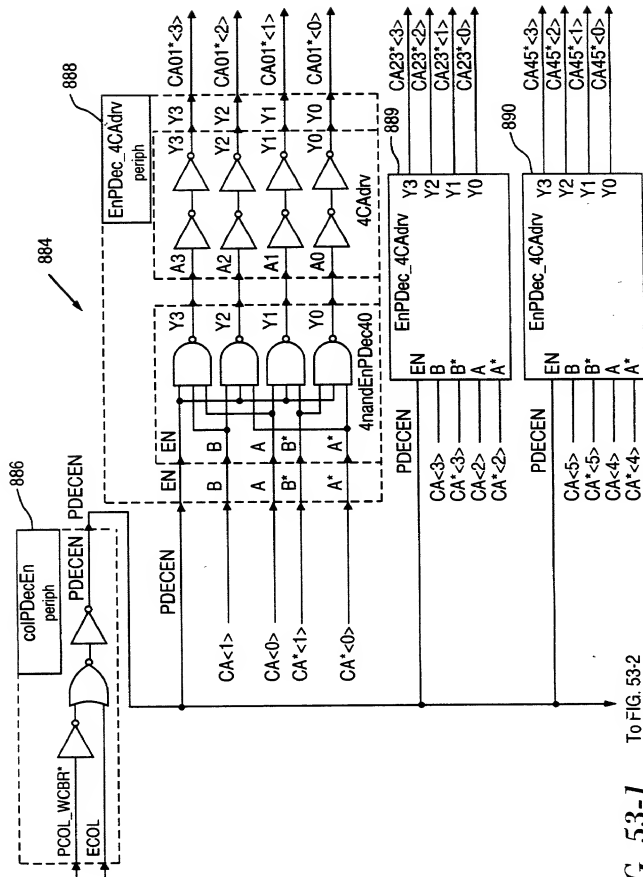


FIG. 53-1 To FIG. 53-2

To FIG. 53-1

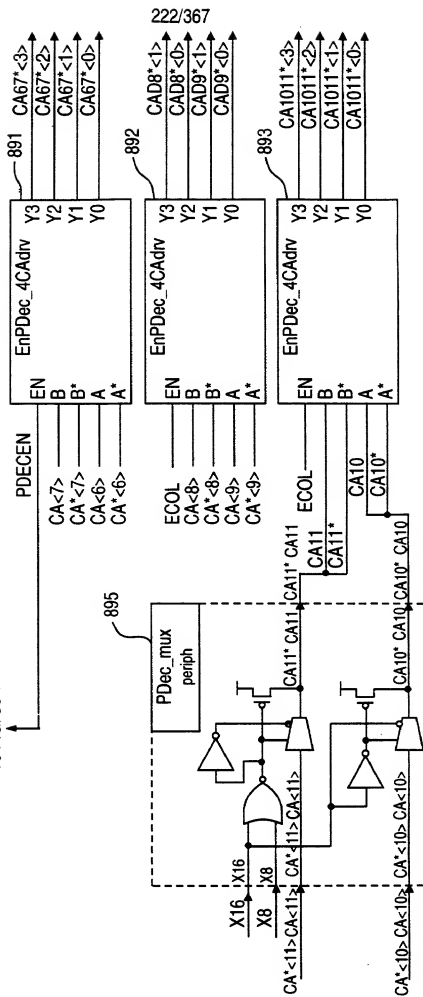


FIG. 53-2

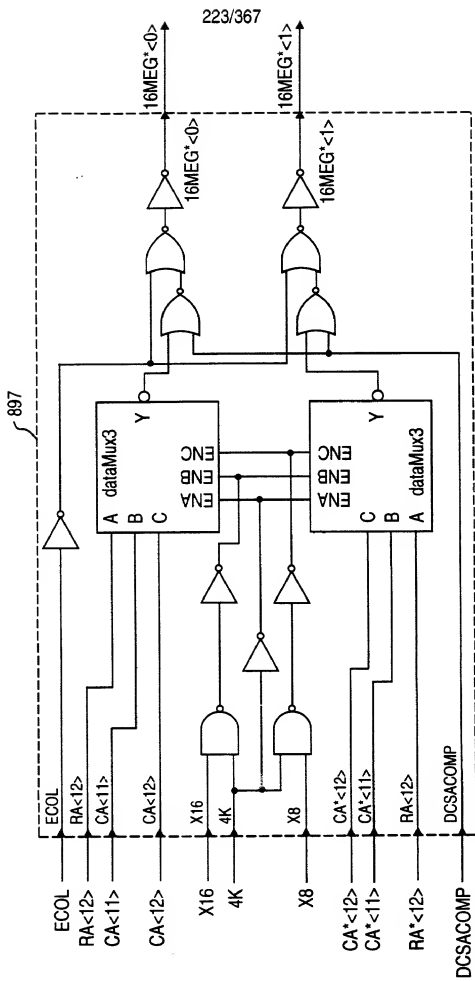


FIG. 54A

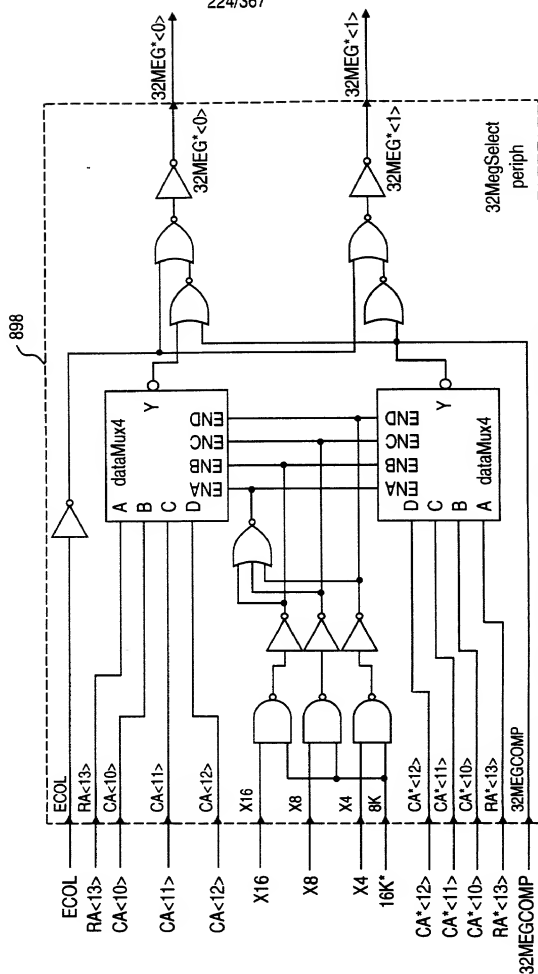


FIG. 54B

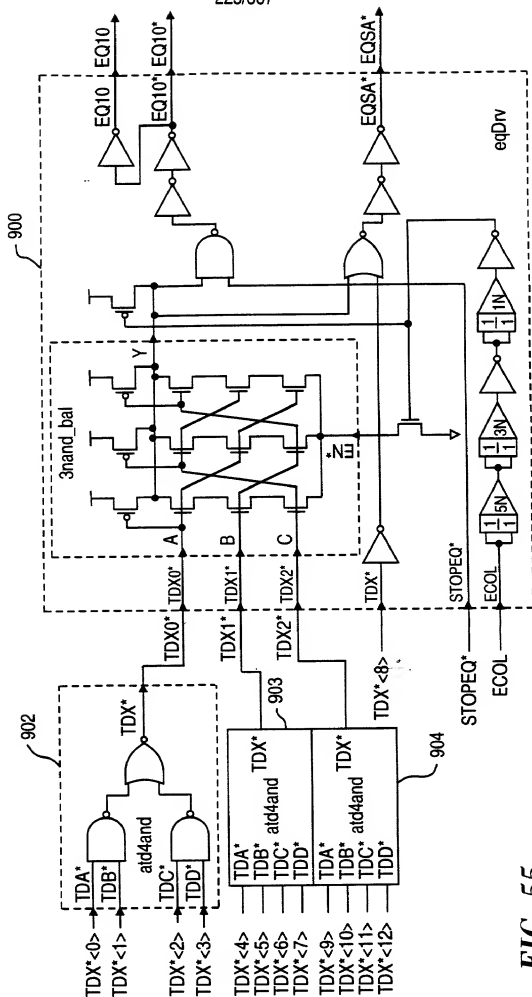


FIG. 55

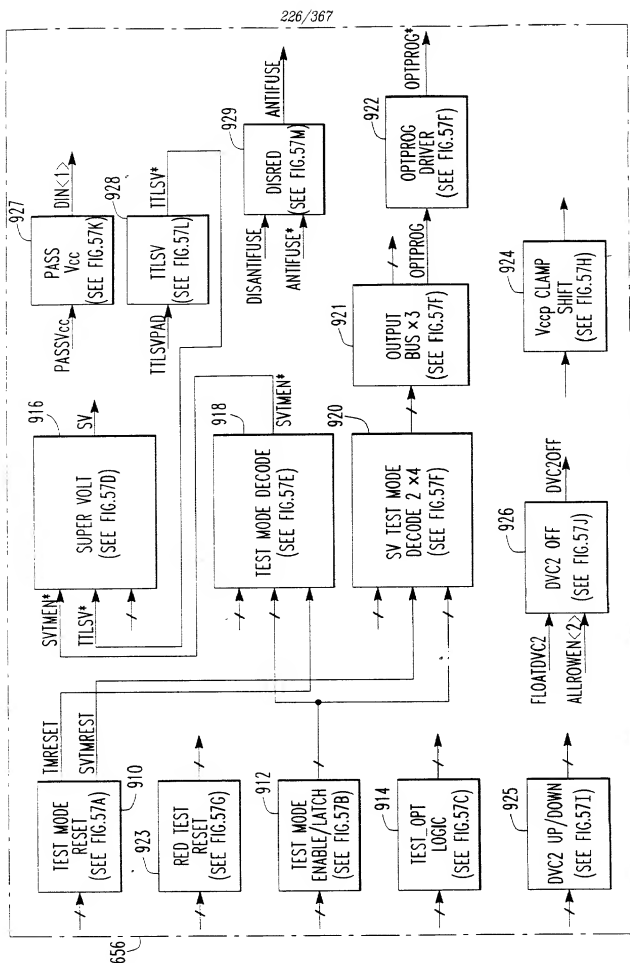


FIG. 56

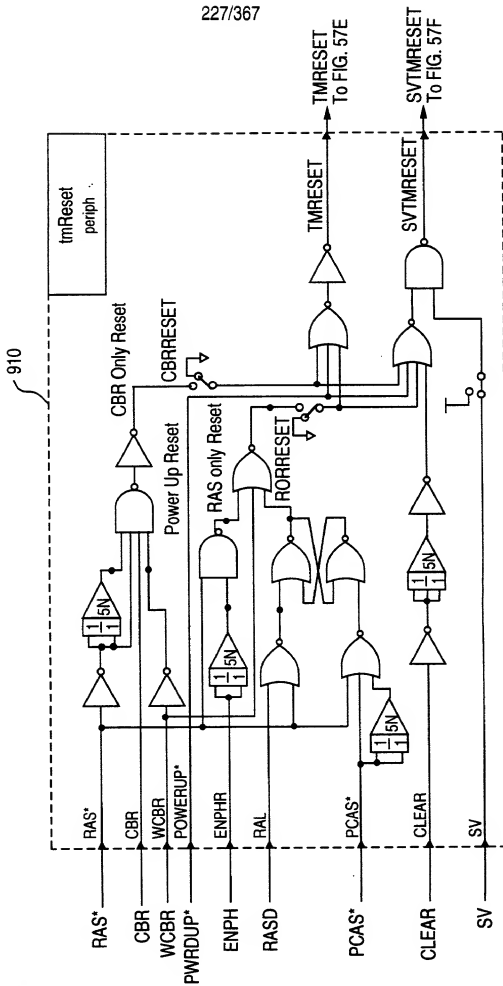


FIG. 57A

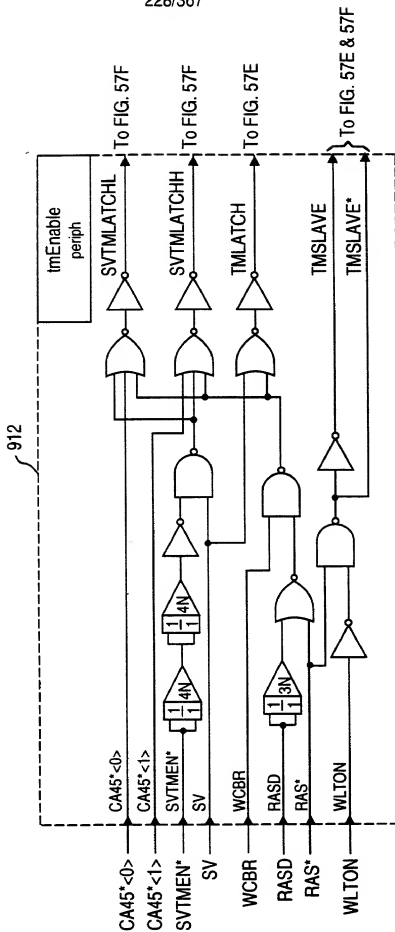


FIG. 57B

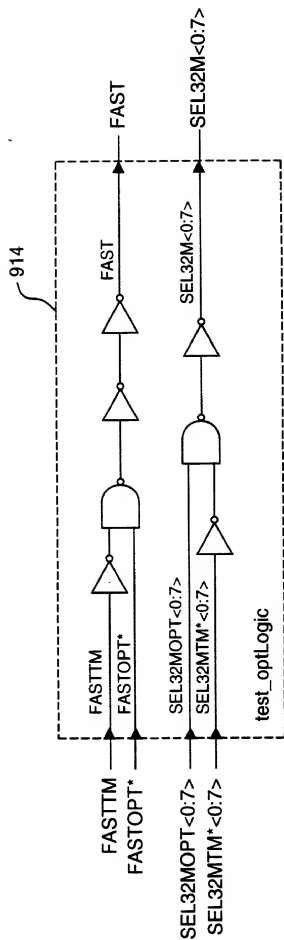


FIG. 57C

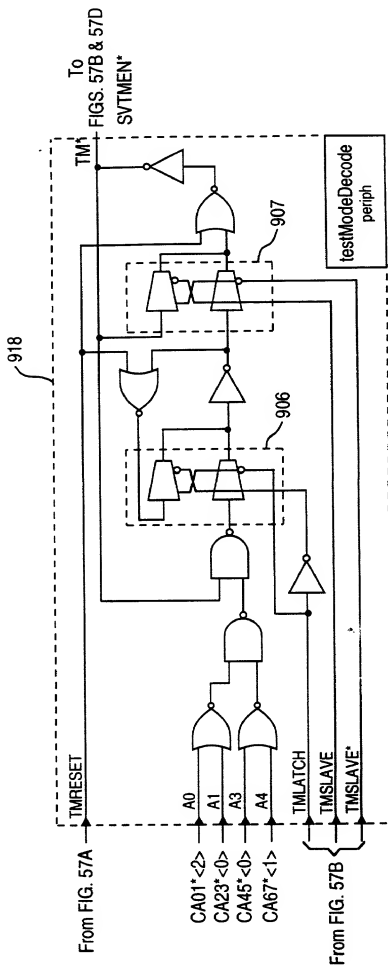


FIG. 57E

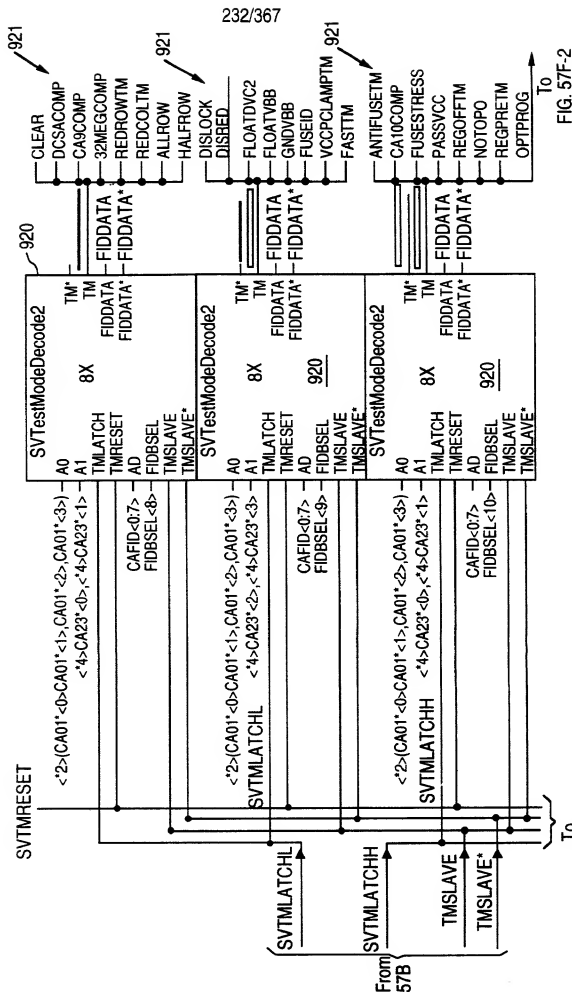


FIG. 57F-1

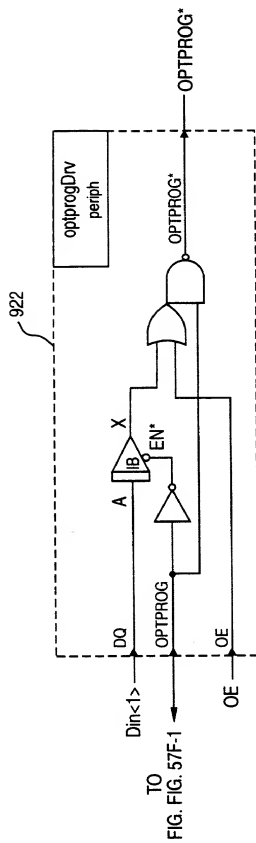


FIG. 57F-2

FIG. 57F-1

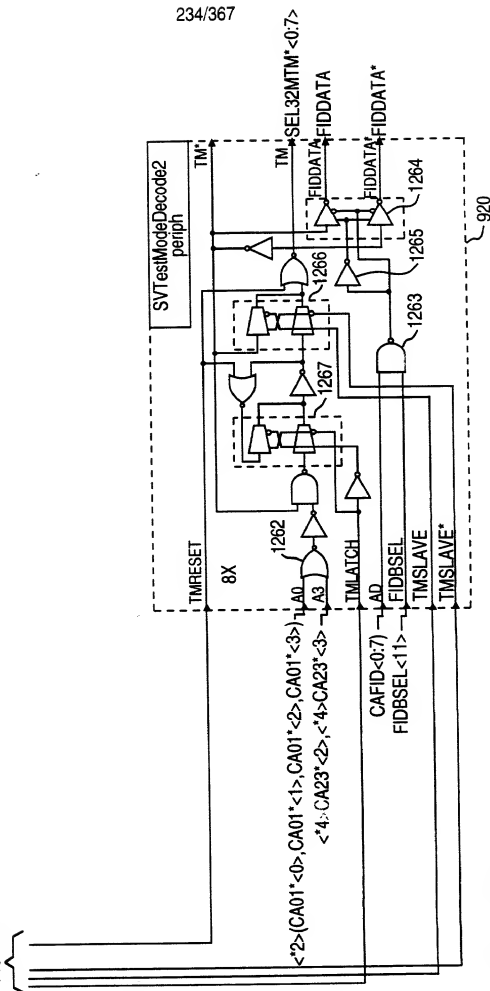


FIG. 57F-3

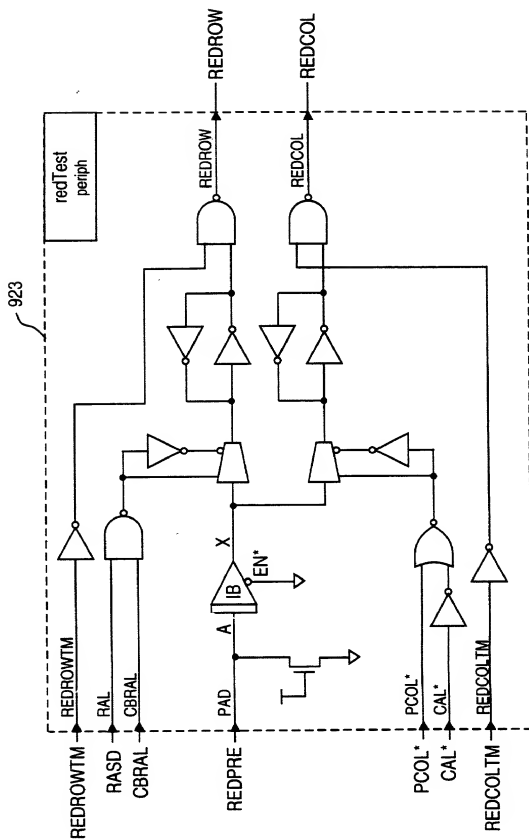
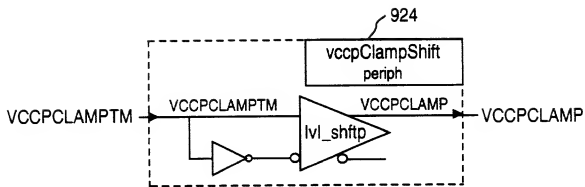
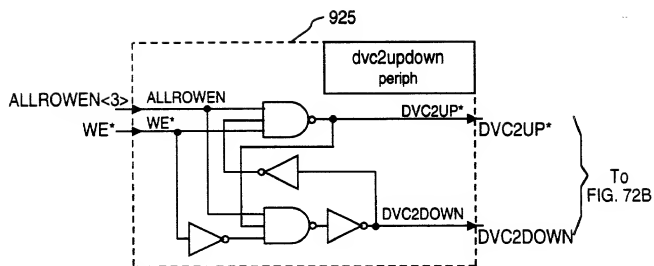
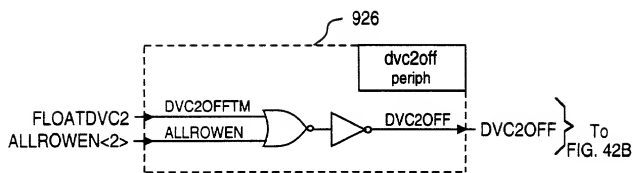
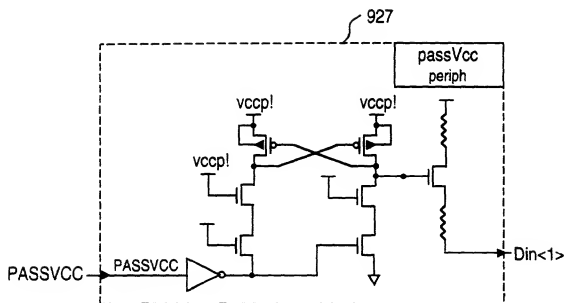


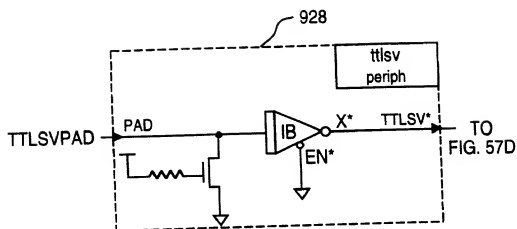
FIG. 57G

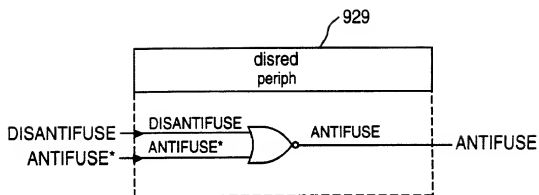
**FIG. 57H**

**FIG. 57I**

**FIG. 57J**

**FIG. 57K**

**FIG. 57L**

**FIG. 57M**

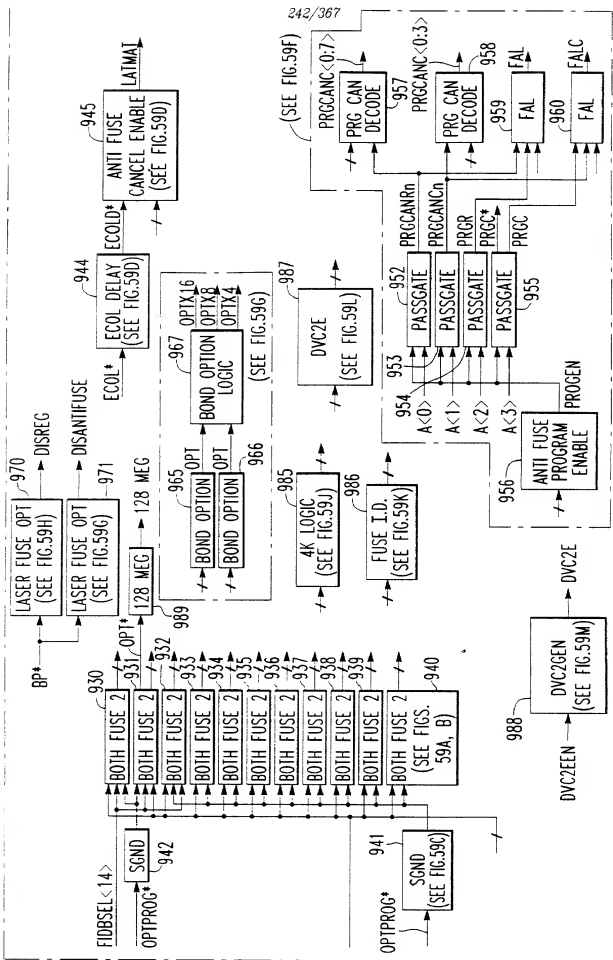


FIG. 58A

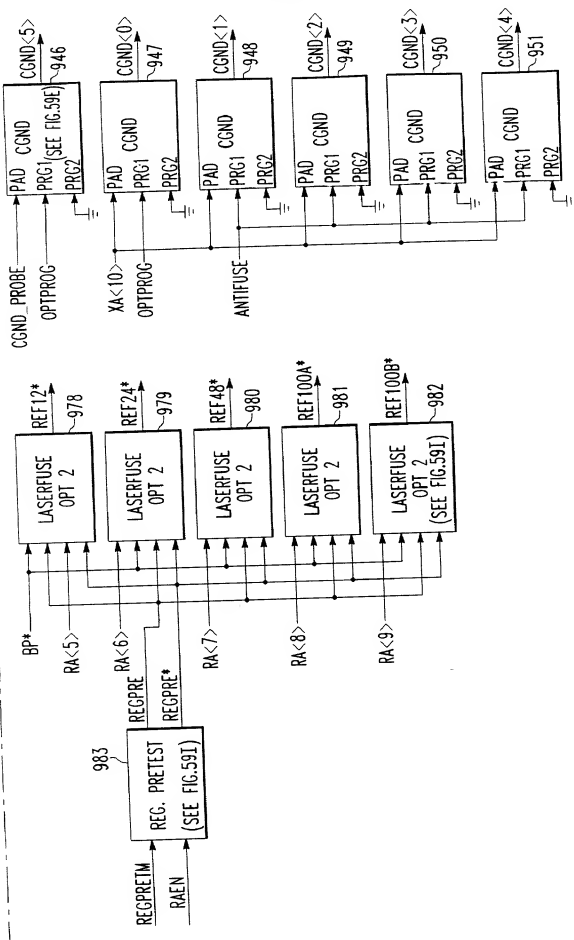


FIG. 58B

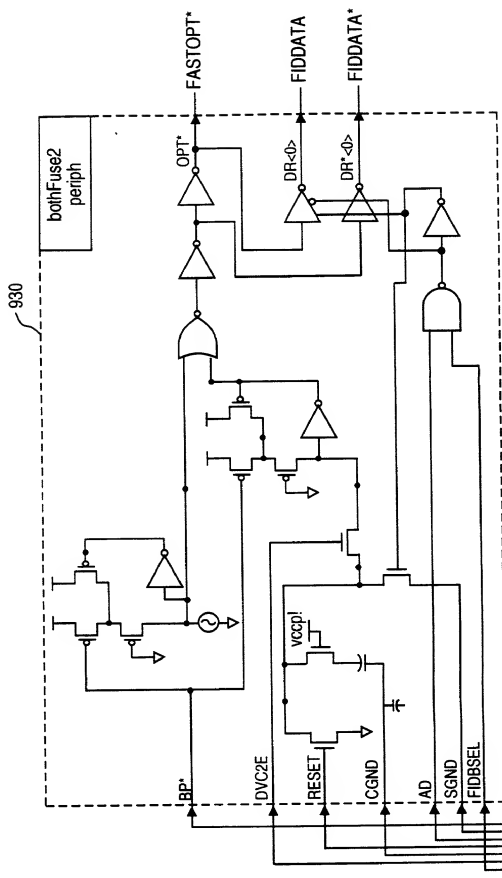


FIG. 59B

FIG. 59A

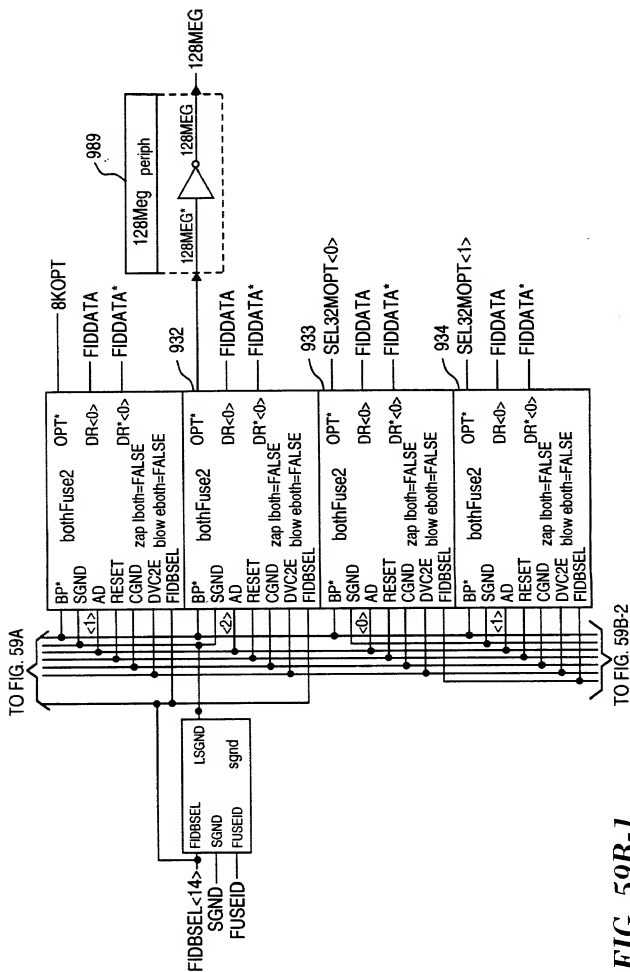


FIG. 59B-1

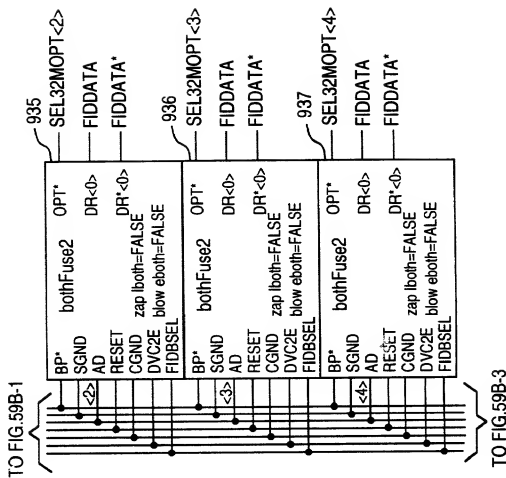


FIG. 59B-2

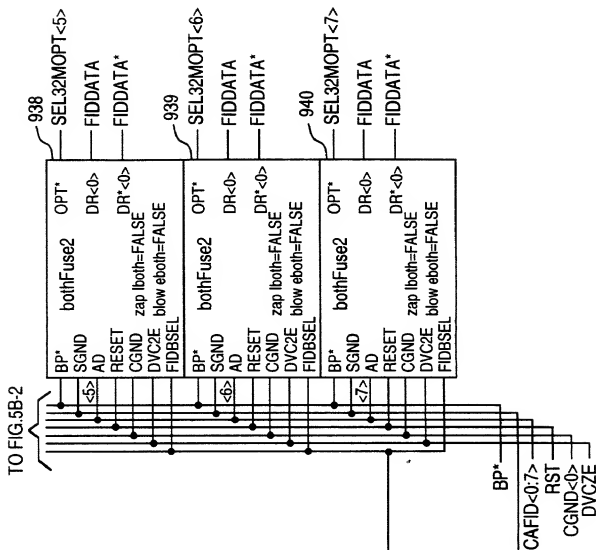
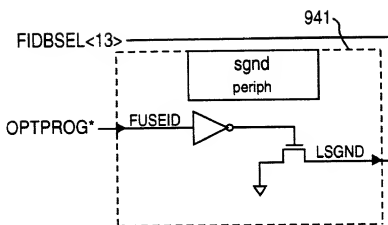
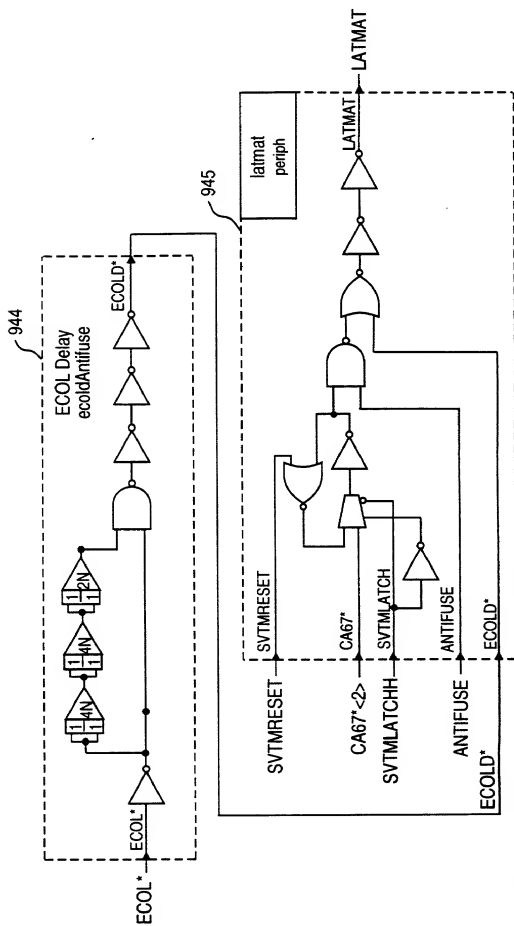


FIG. 59B-3

**FIG. 59C**



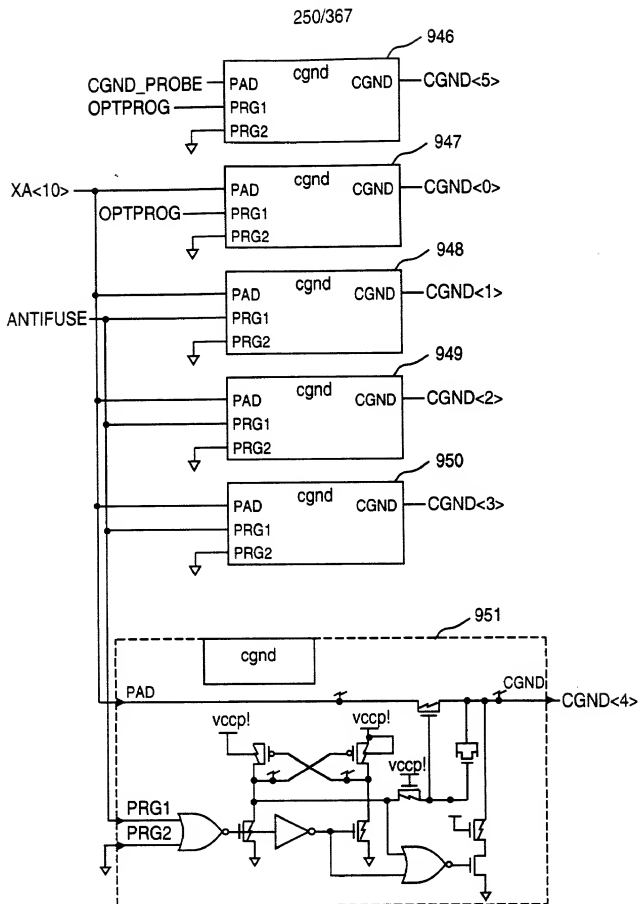


FIG. 59E

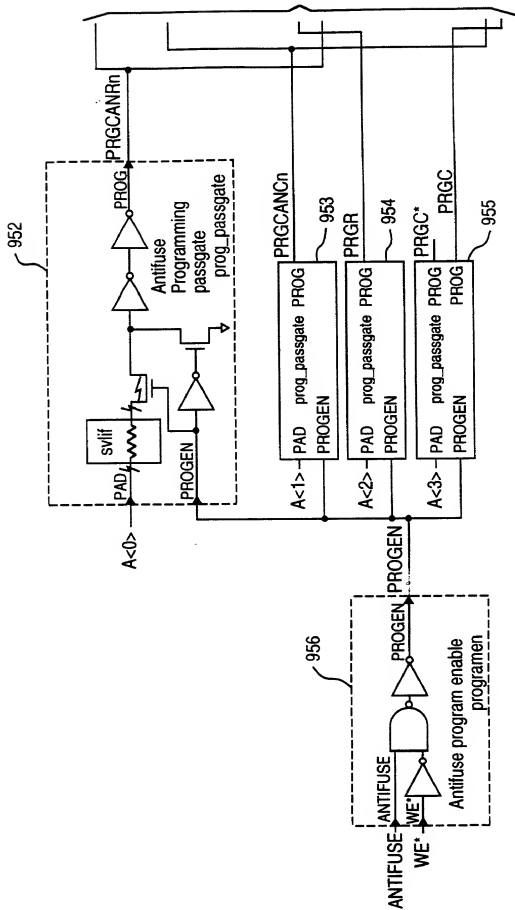


FIG. 59F-1

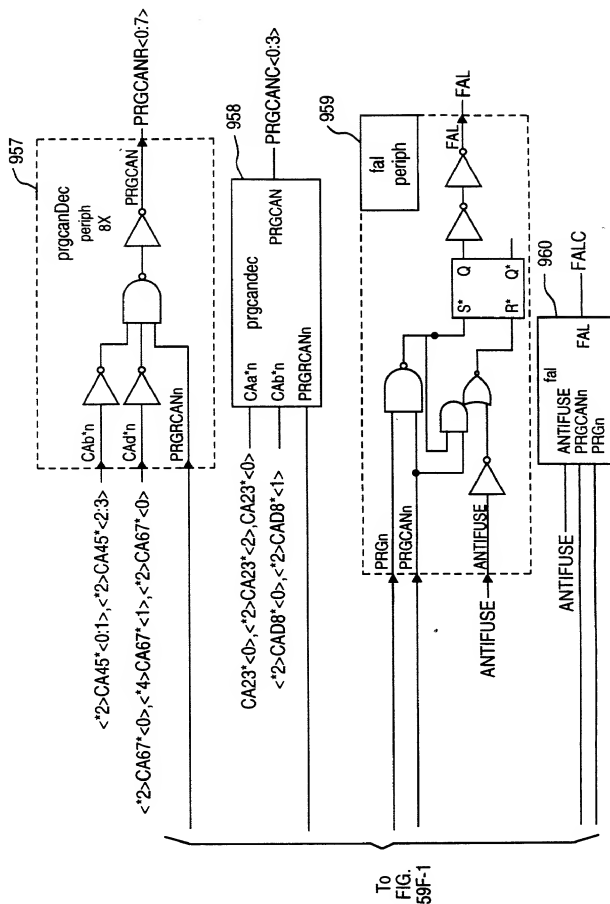
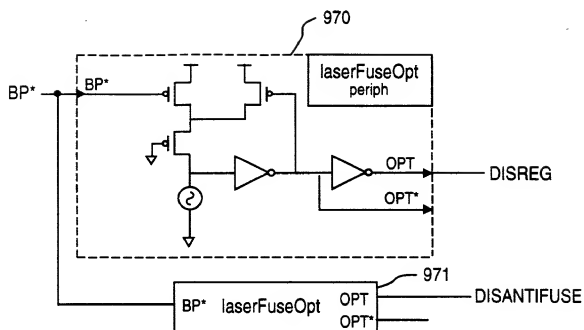


FIG. 59F-2

**FIG. 59H**

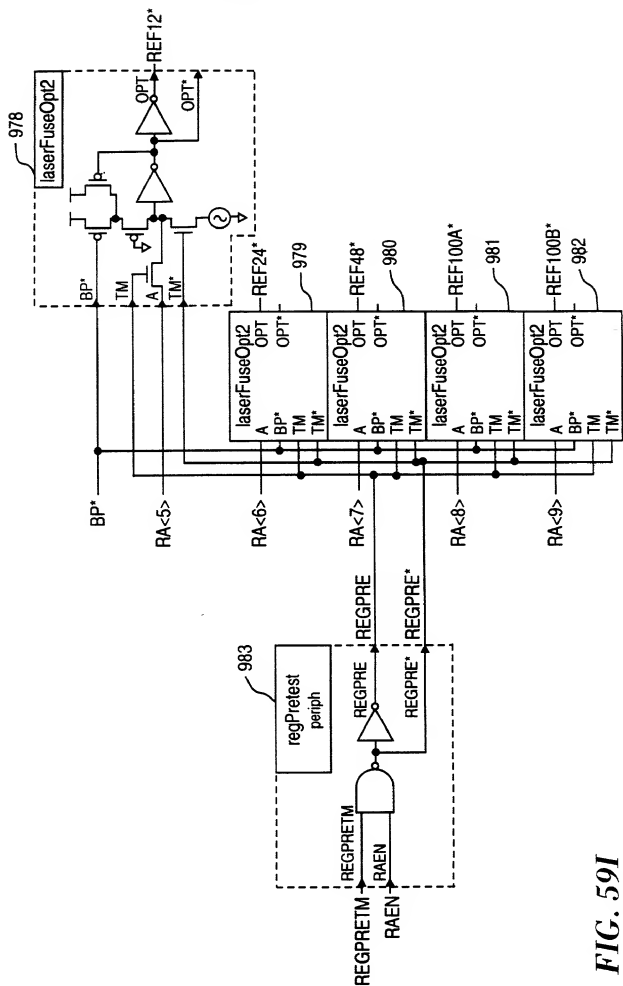


FIG. 591

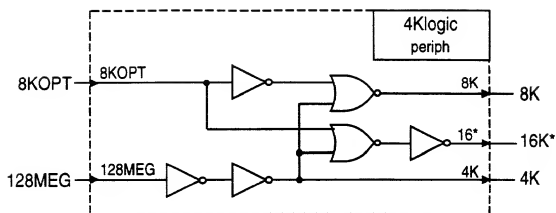
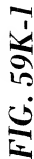
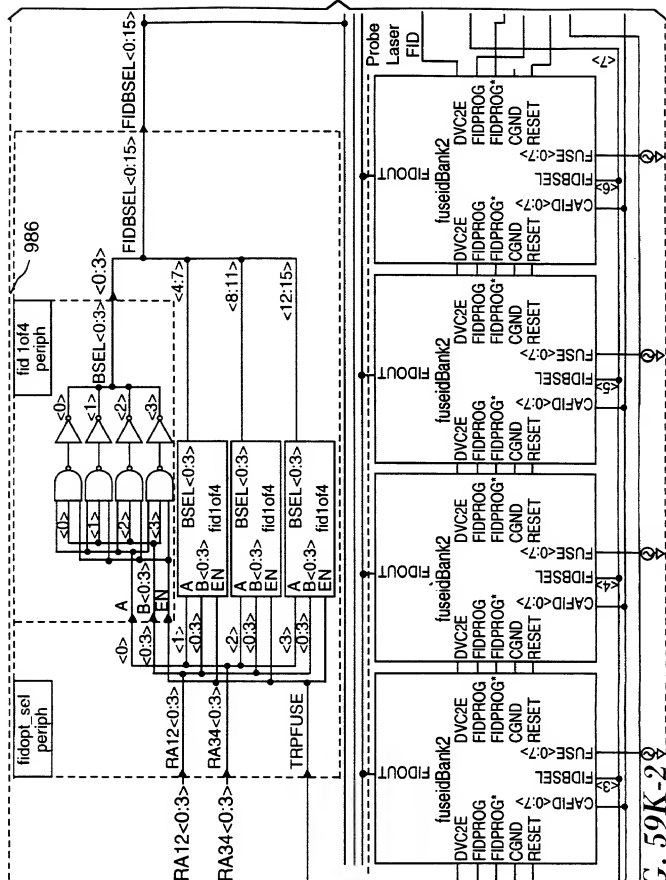


FIG. 59J





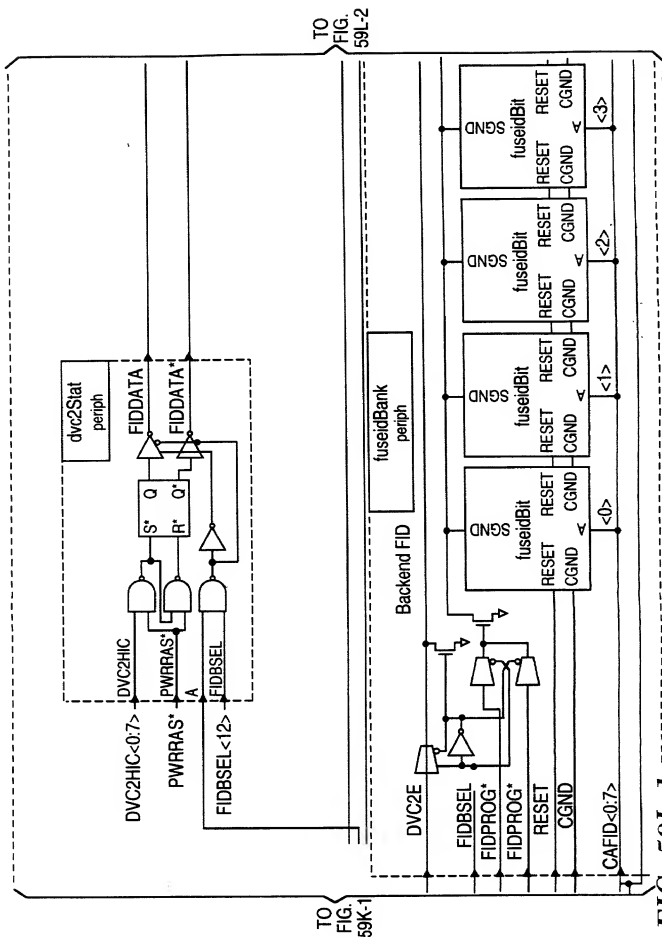


FIG. 59L-1

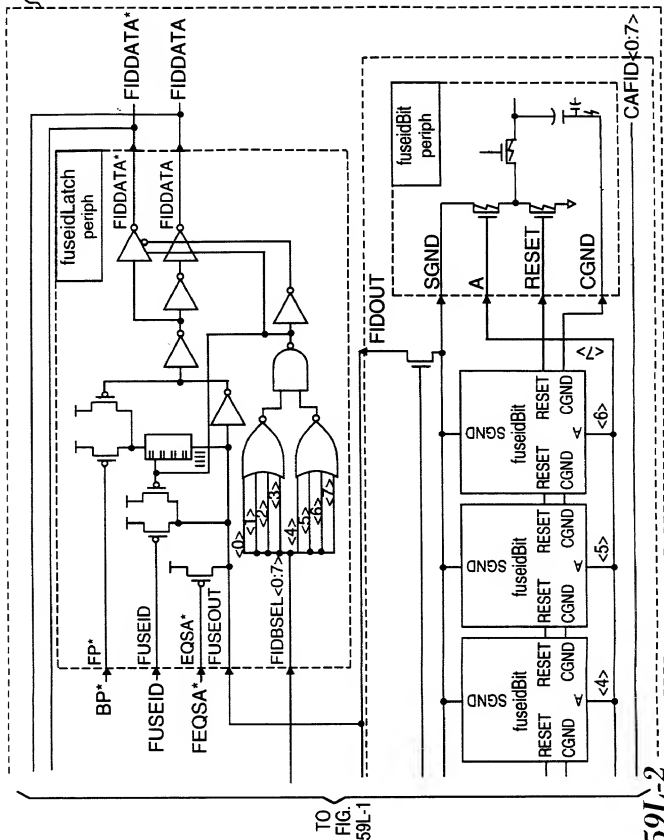


FIG. 59L-2

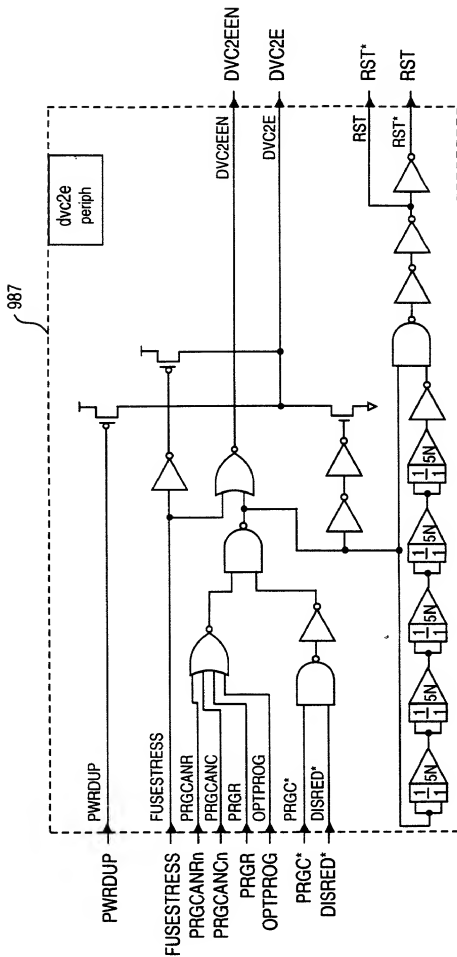
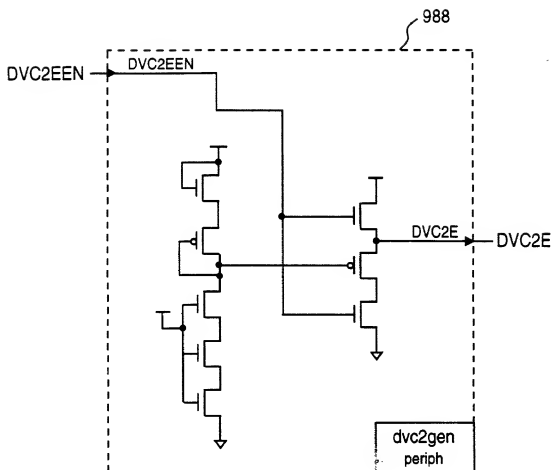
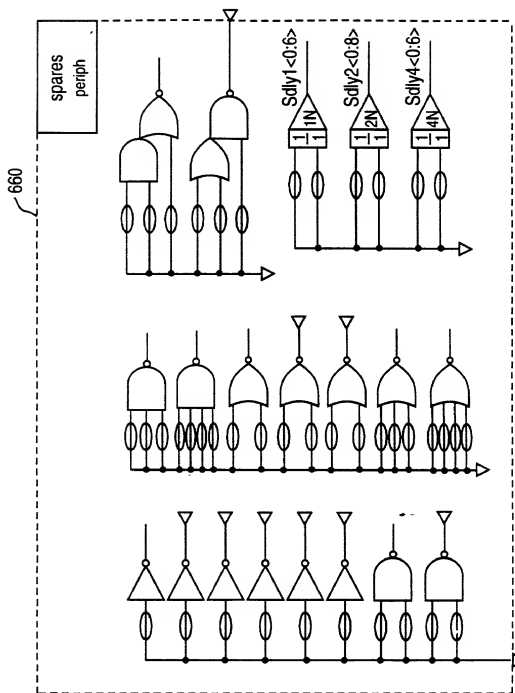


FIG. 59M

**FIG. 59N**



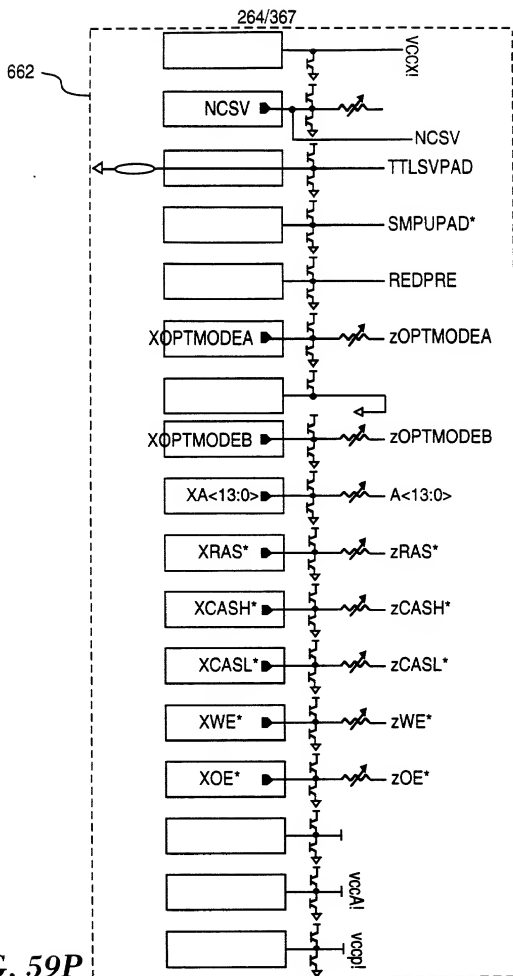


FIG. 59P

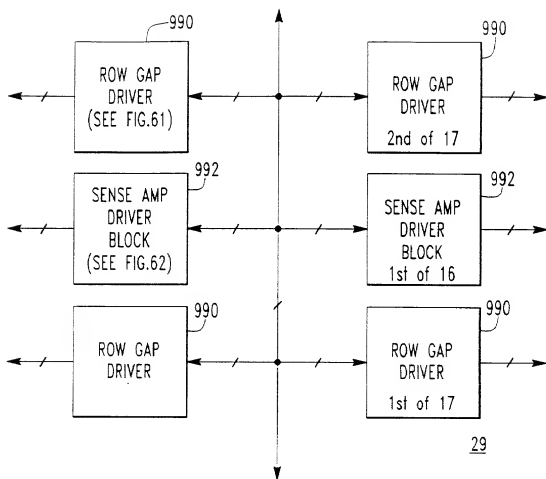


FIG. 60

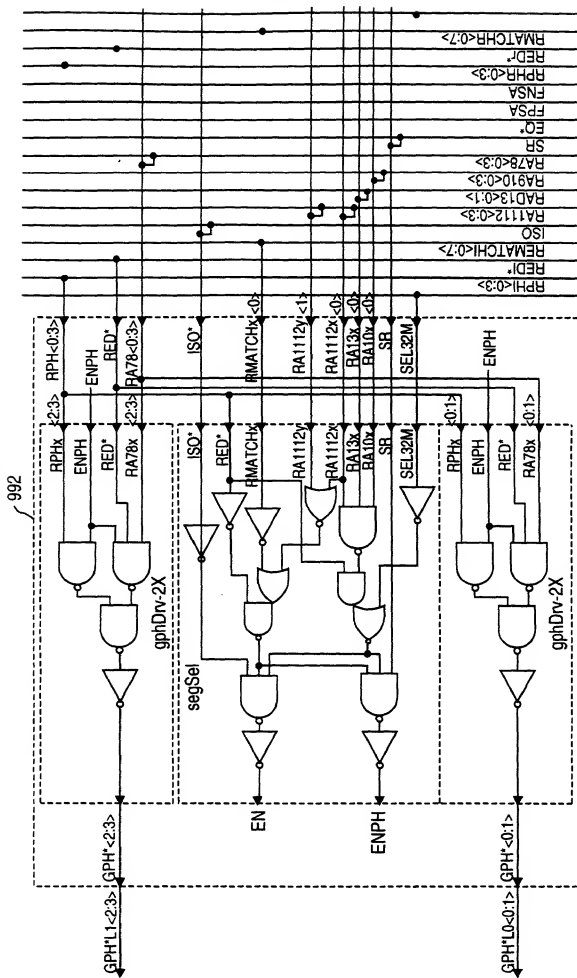


FIG. 61

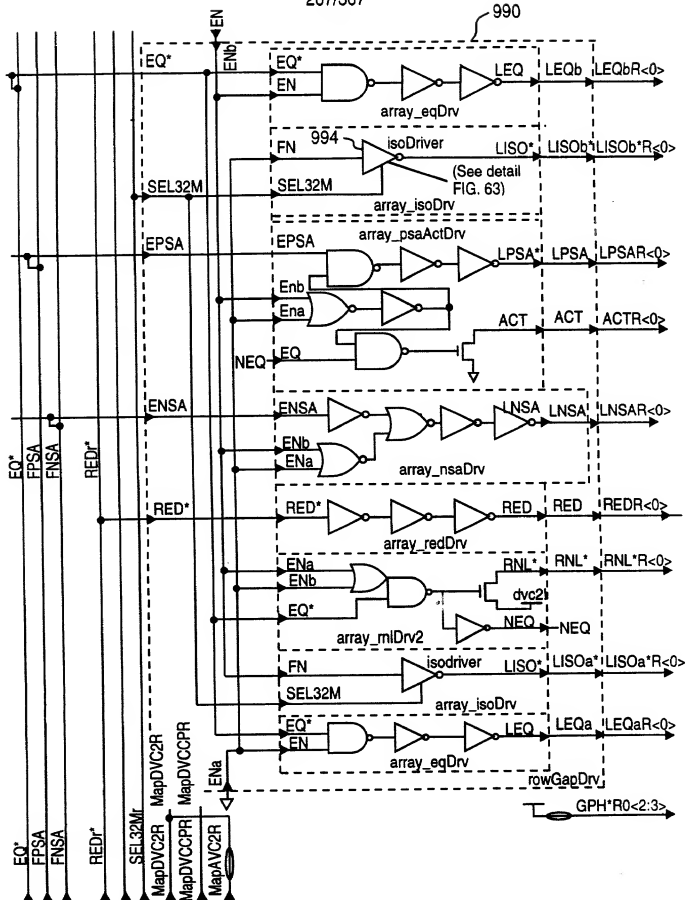


FIG. 62

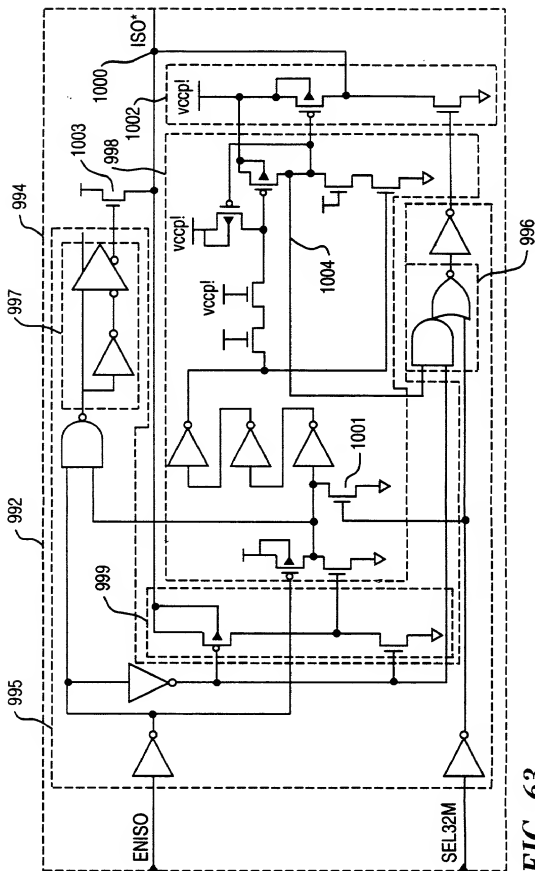


FIG. 63

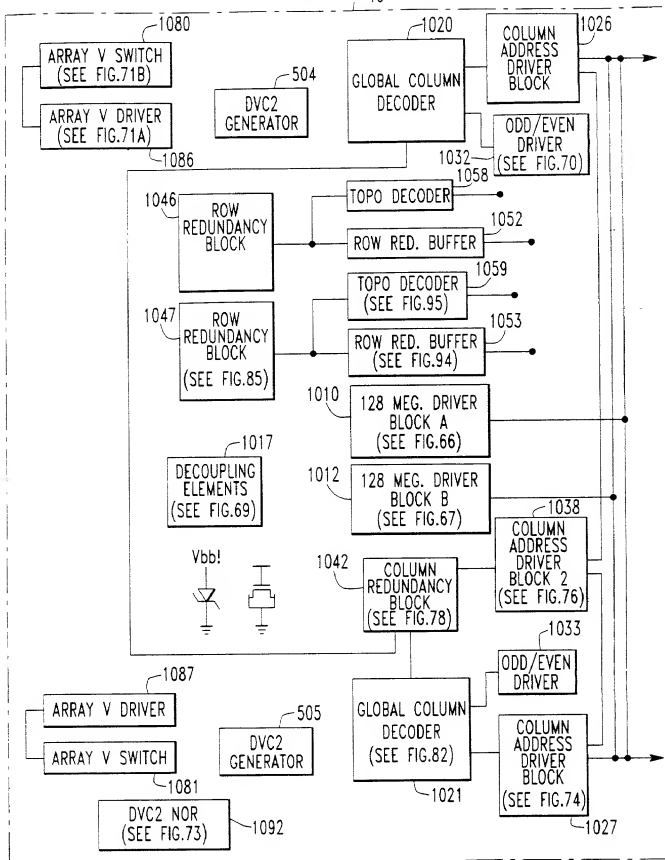


FIG. 64A

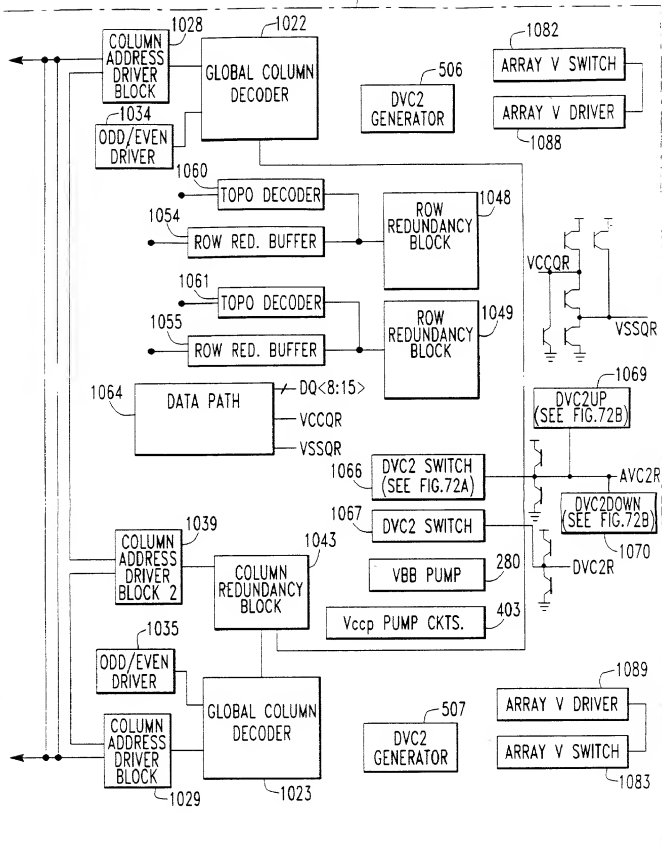


FIG. 64B

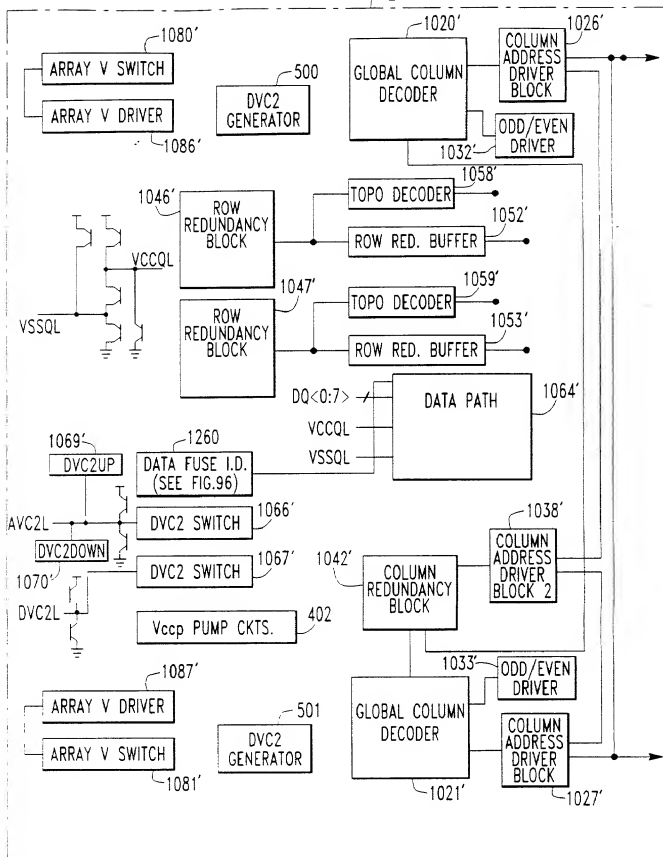


FIG. 65A

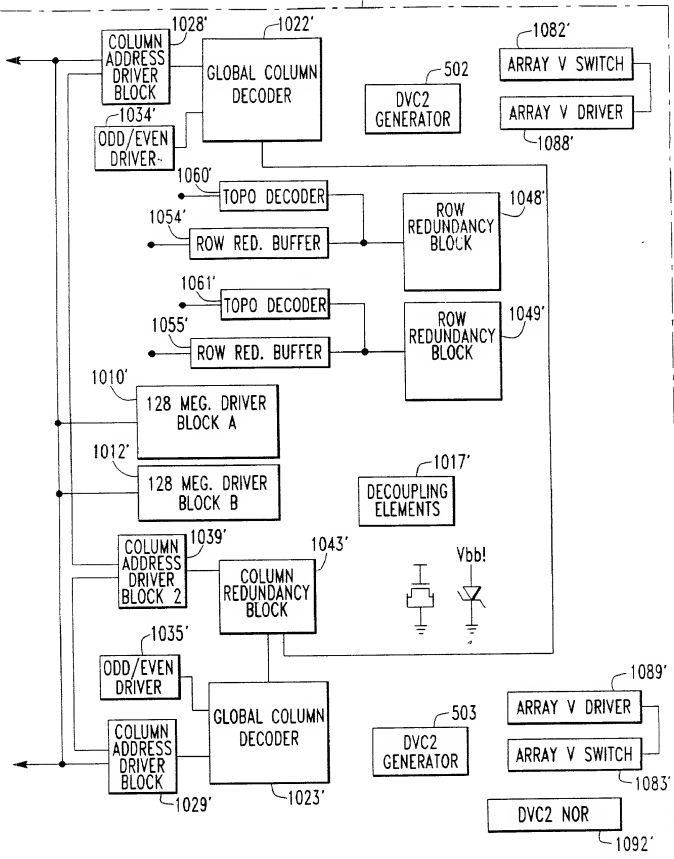


FIG. 65B

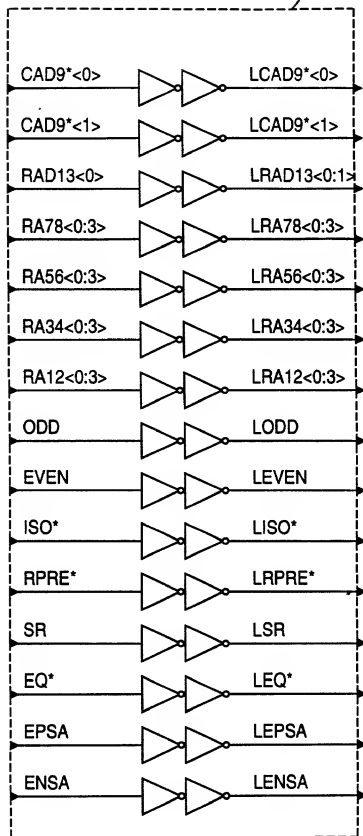


FIG. 66

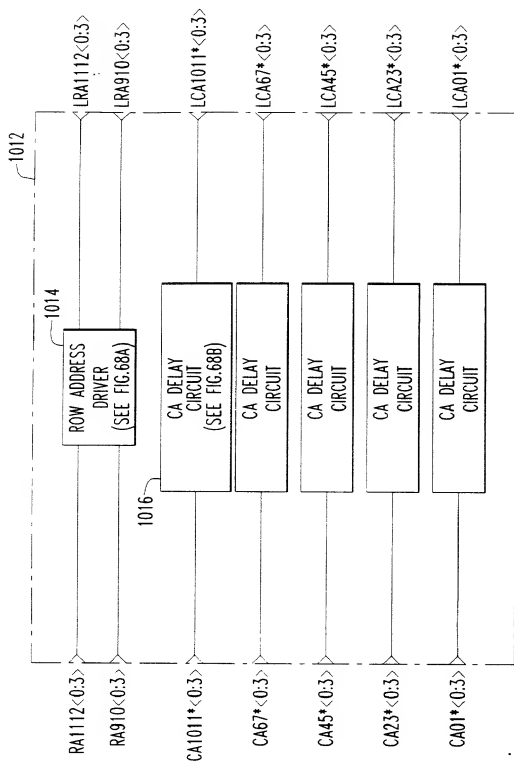
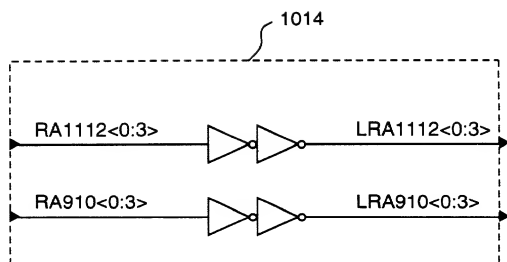
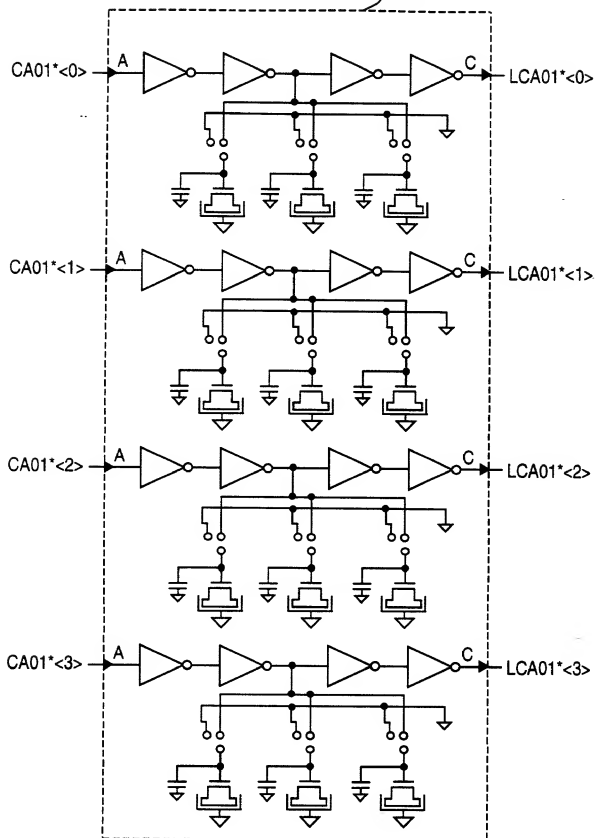
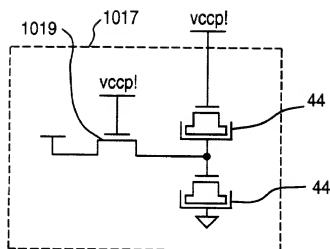
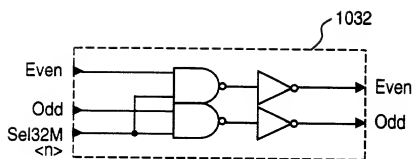


FIG. 67

**FIG. 68A**

**FIG. 68B**

**FIG. 69**

**FIG. 70**

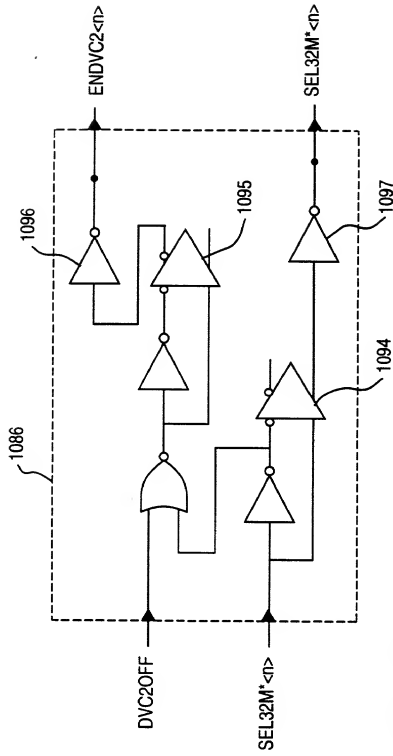
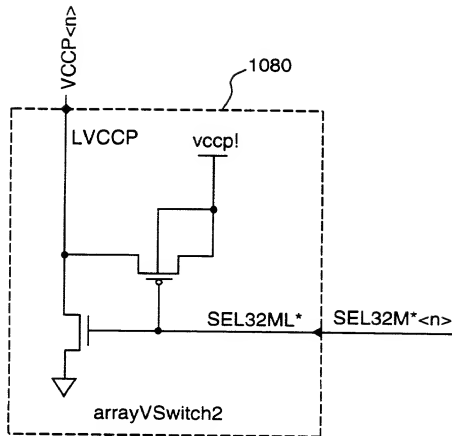


FIG. 71A

**FIG. 71B**

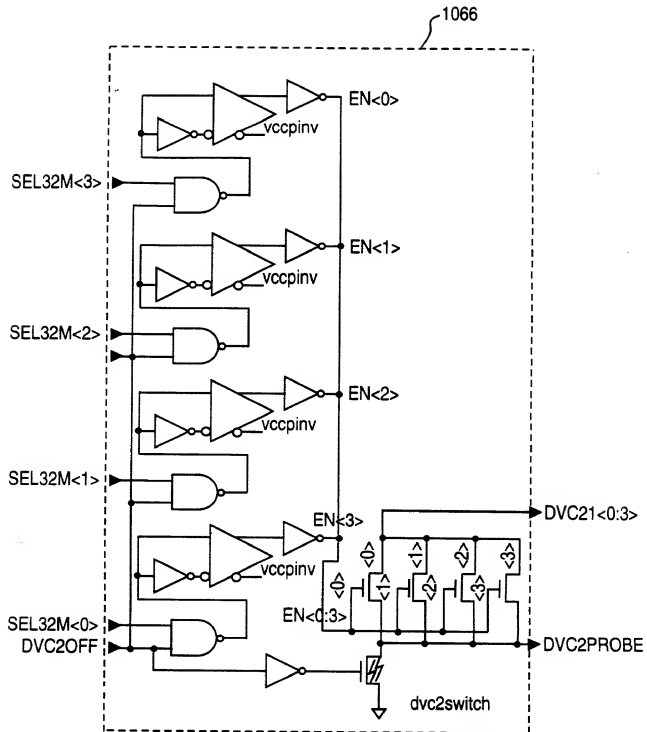
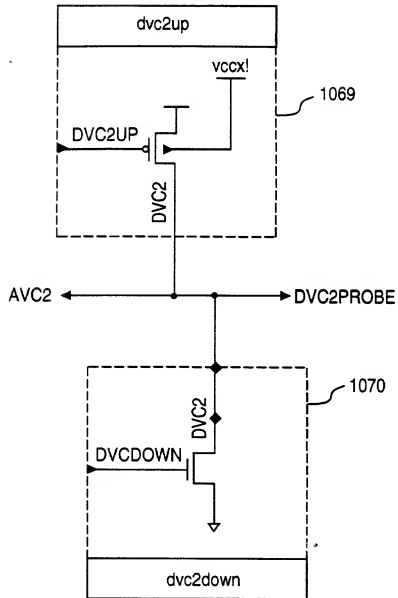
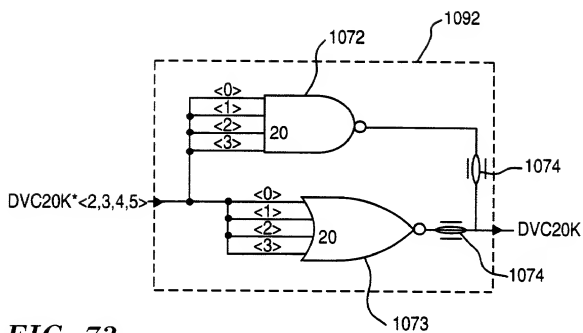


FIG. 72A

**FIG. 72B**

**FIG. 73**

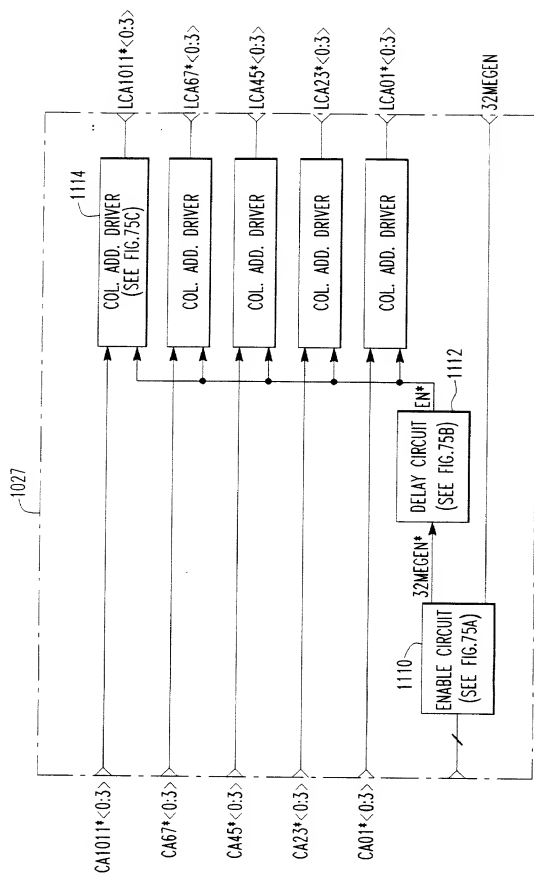


FIG. 74

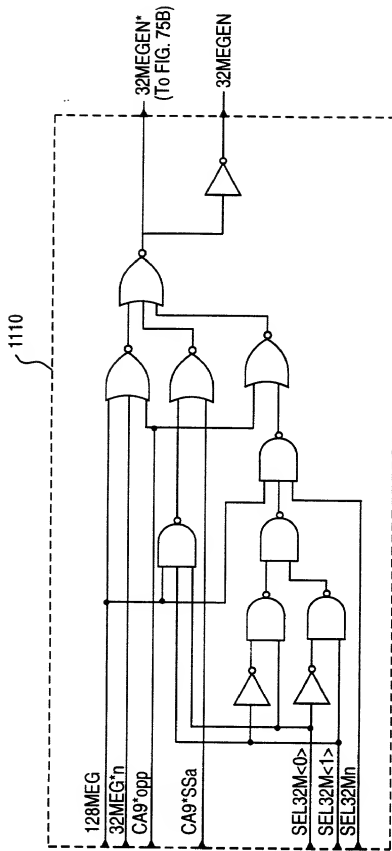


FIG. 75A

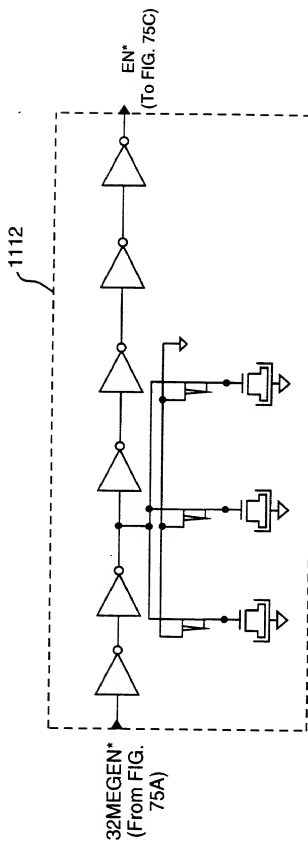


FIG. 75B

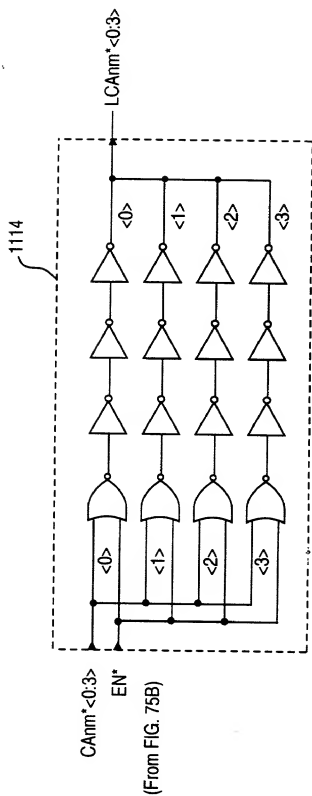


FIG. 75C

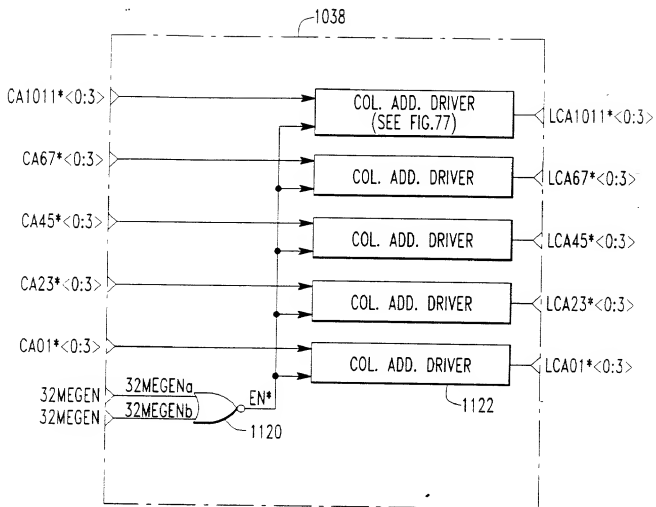


FIG. 76

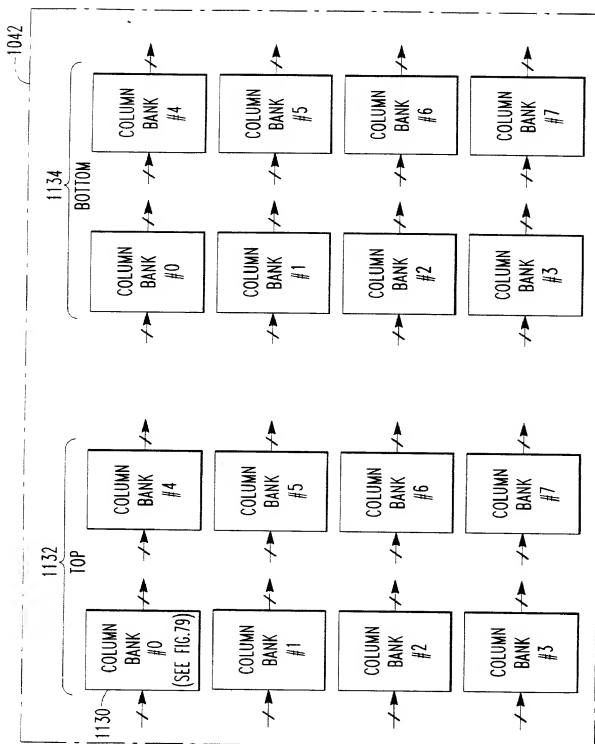


FIG. 78

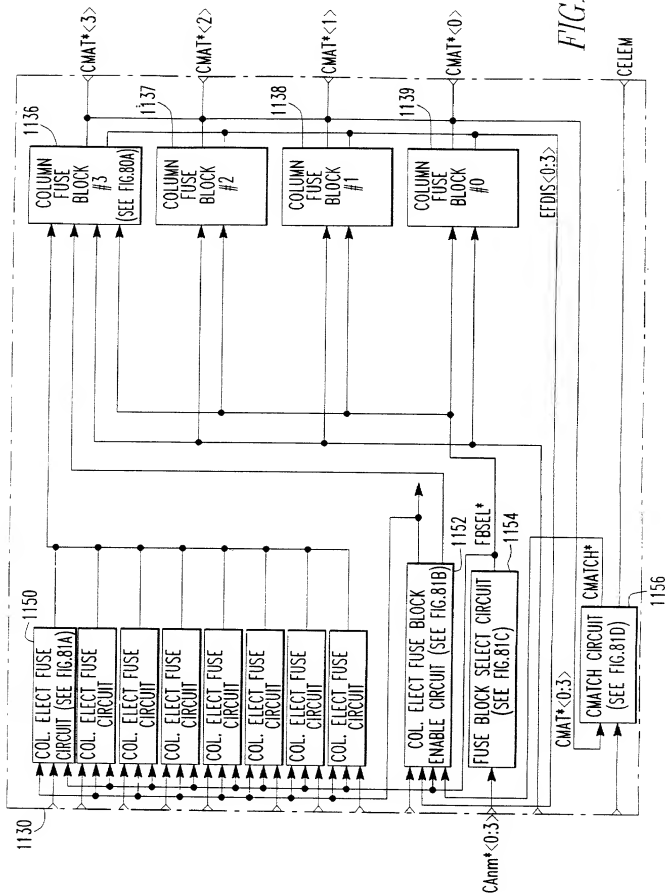


FIG. 79

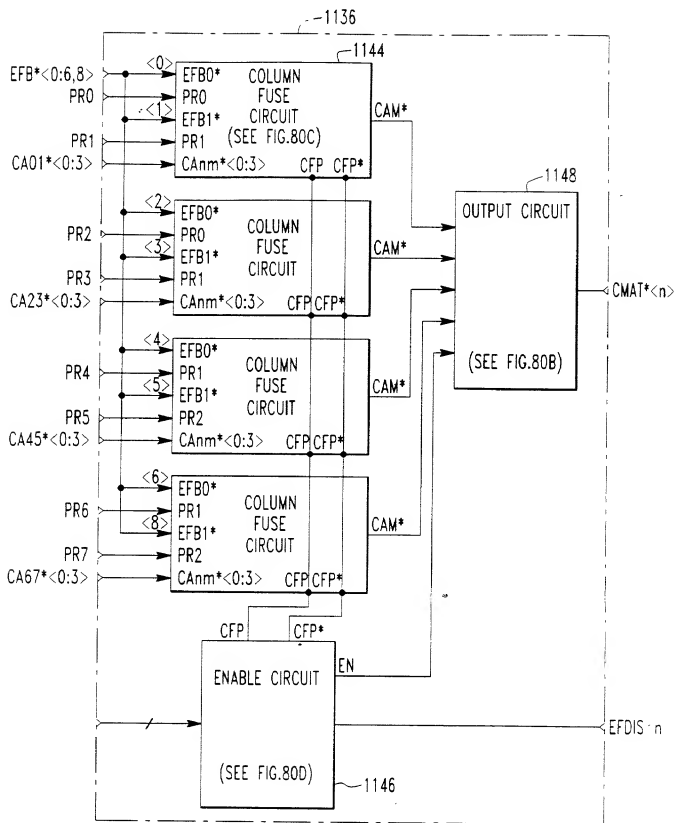
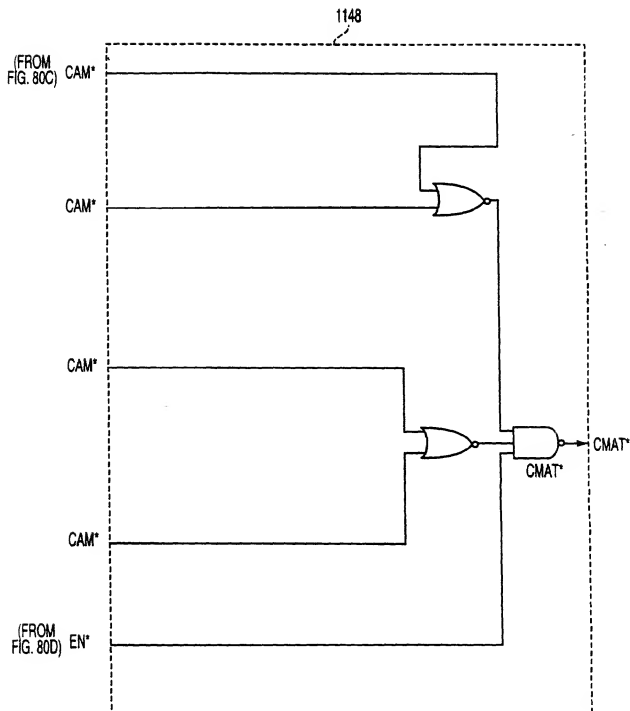


FIG. 80A

**FIG. 80B**

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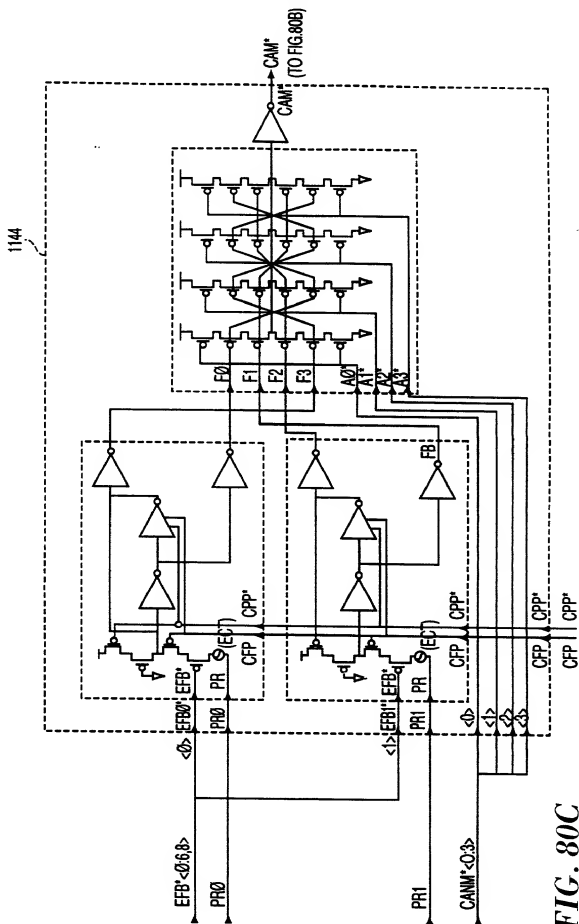
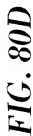


FIG. 80C



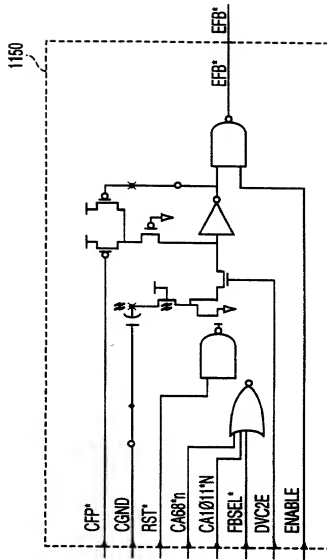


FIG. 81A

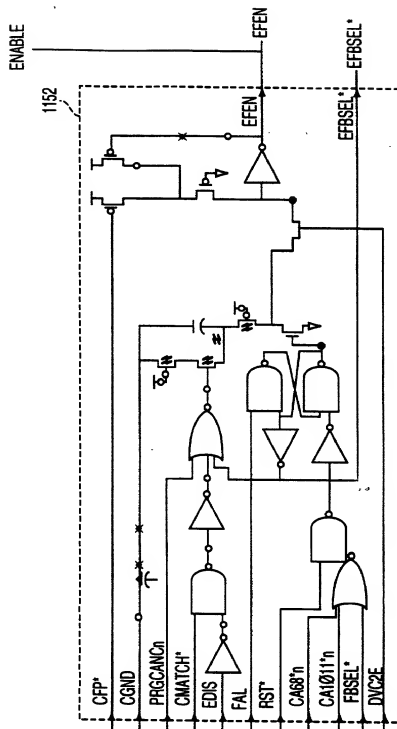


FIG. 81B

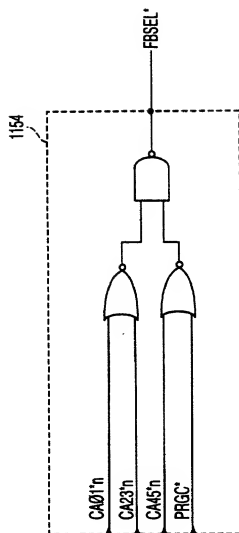


FIG. 81C

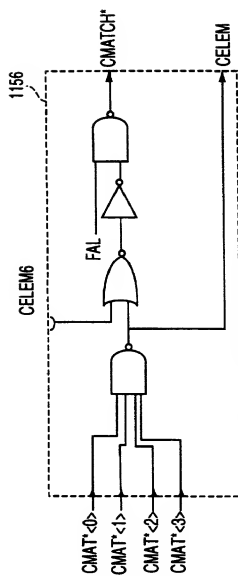


FIG. 81D

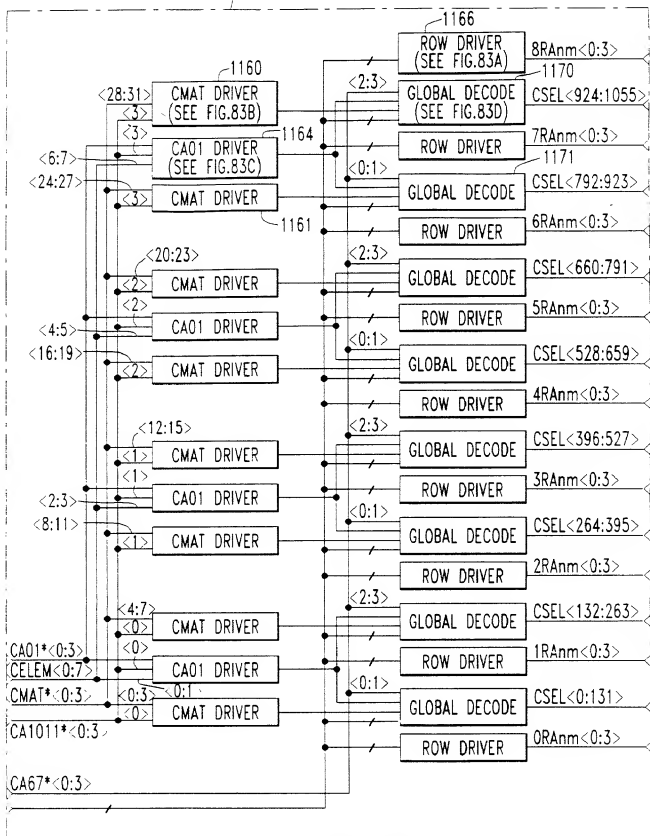


FIG. 82

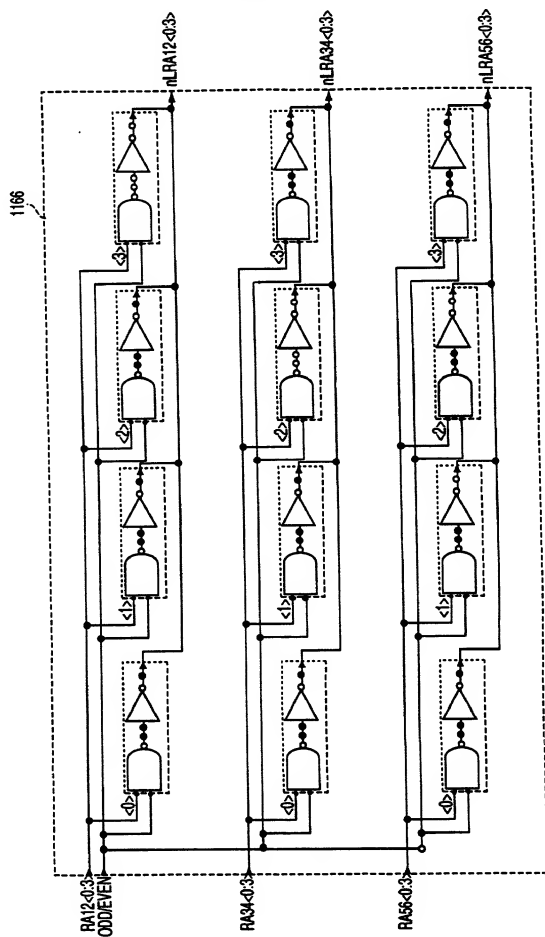


FIG. 83A

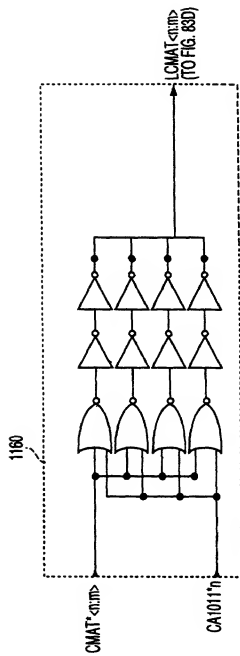


FIG. 83B

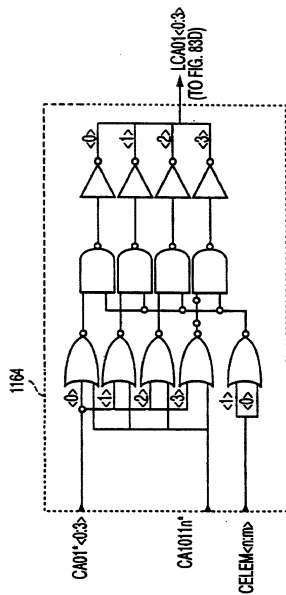
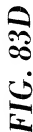


FIG. 83C



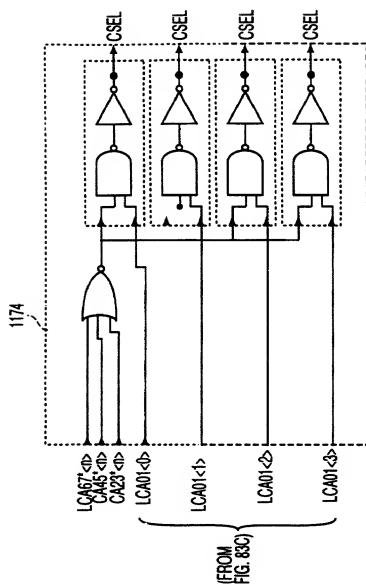
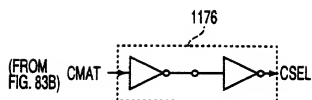


FIG. 84A

**FIG. 84B**

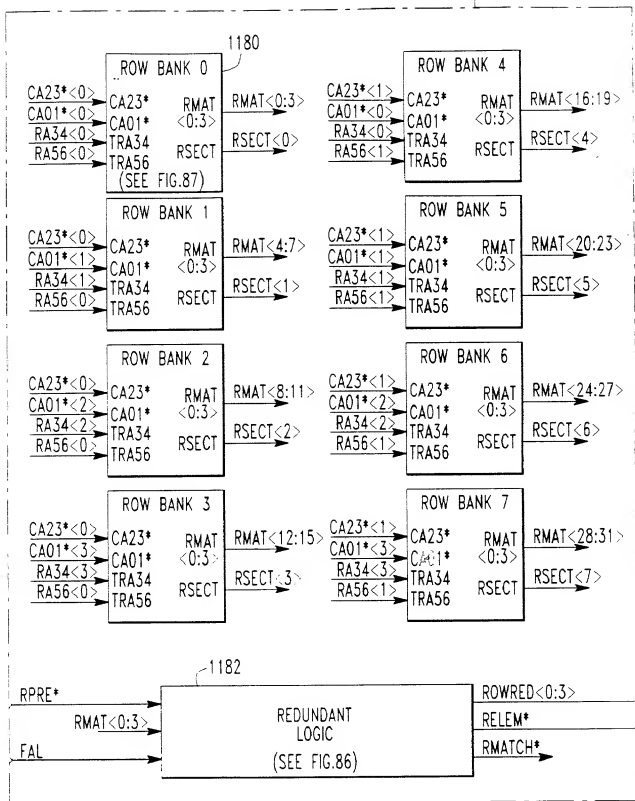


FIG. 85

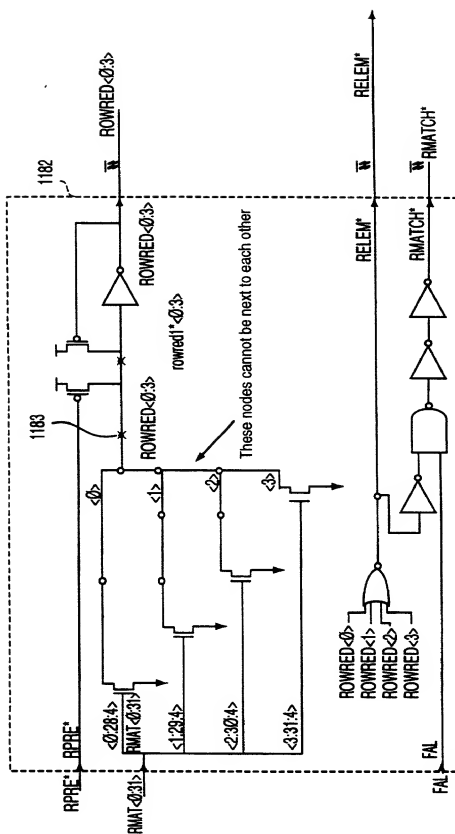


FIG. 86

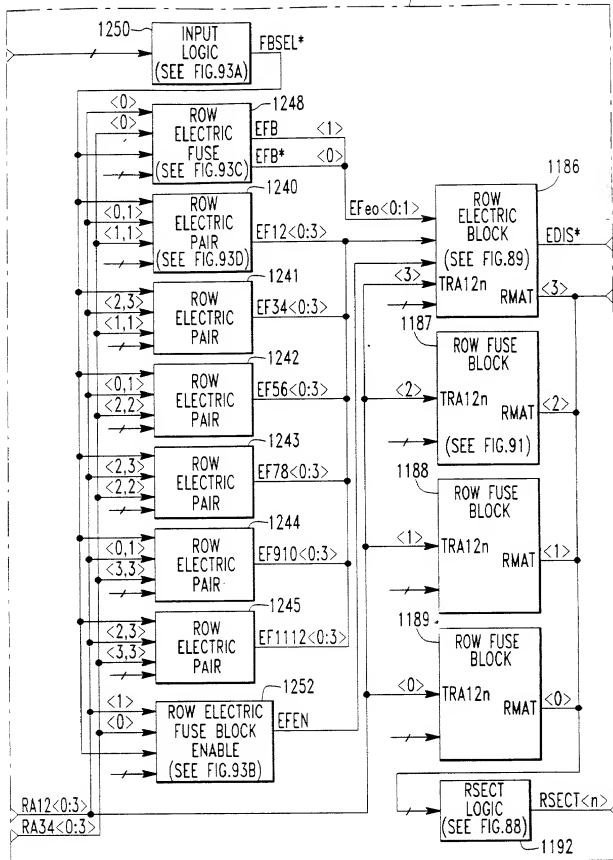
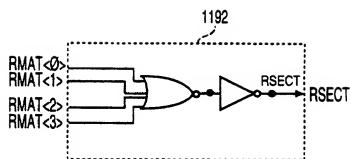
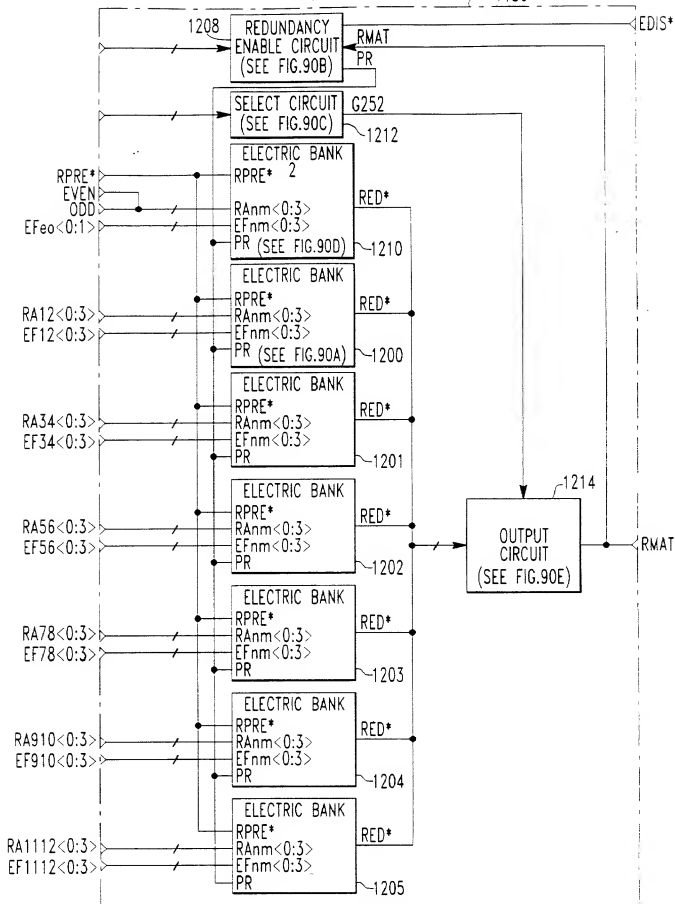


FIG. 87

**FIG. 88**



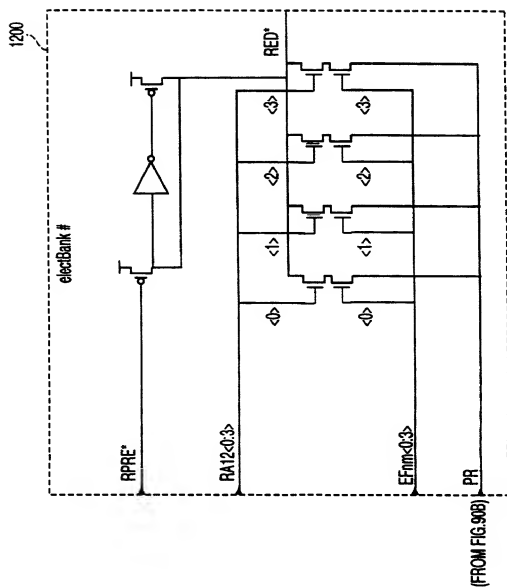


FIG. 90A

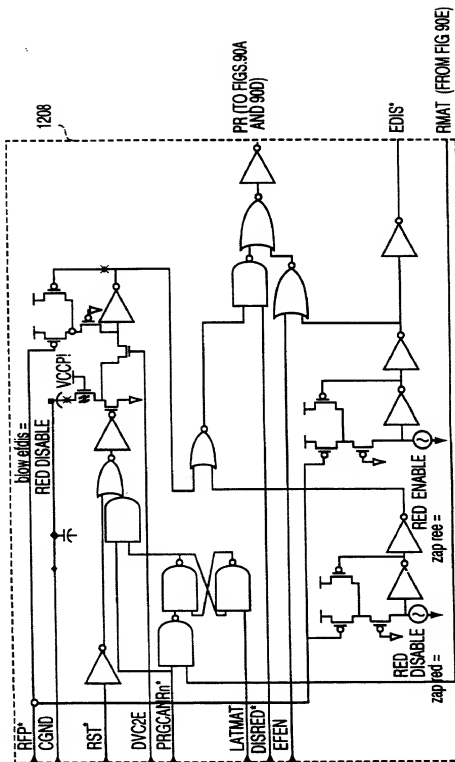
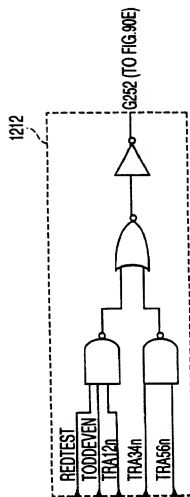


FIG. 90B

**FIG. 90C**

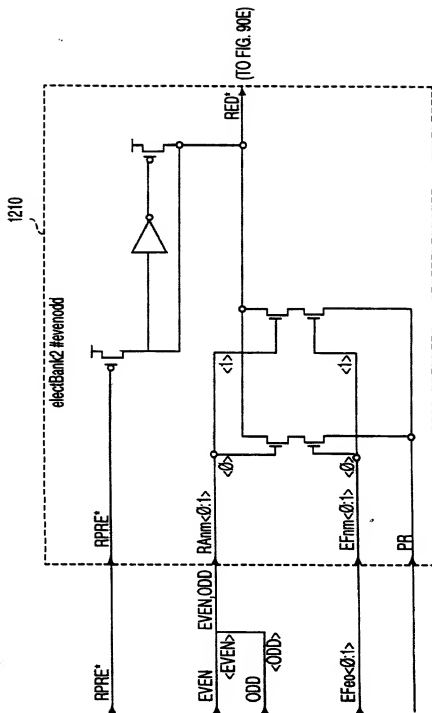


FIG. 90D

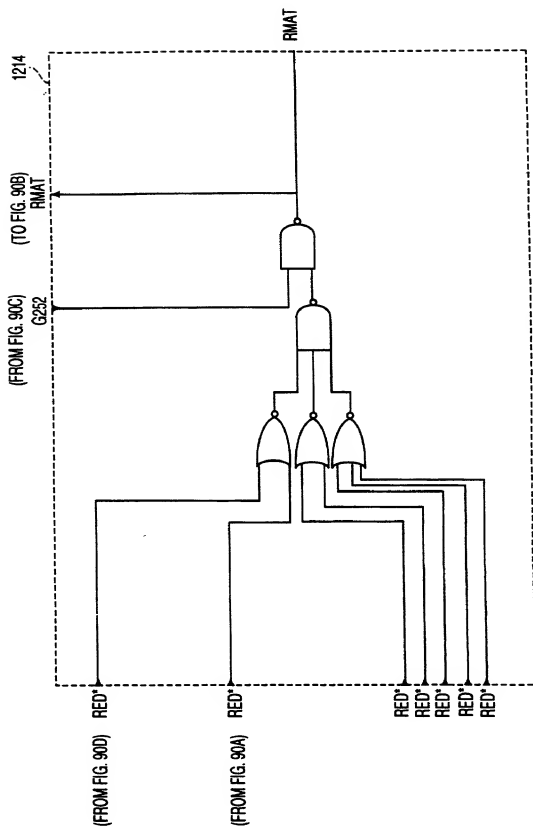


FIG. 90E

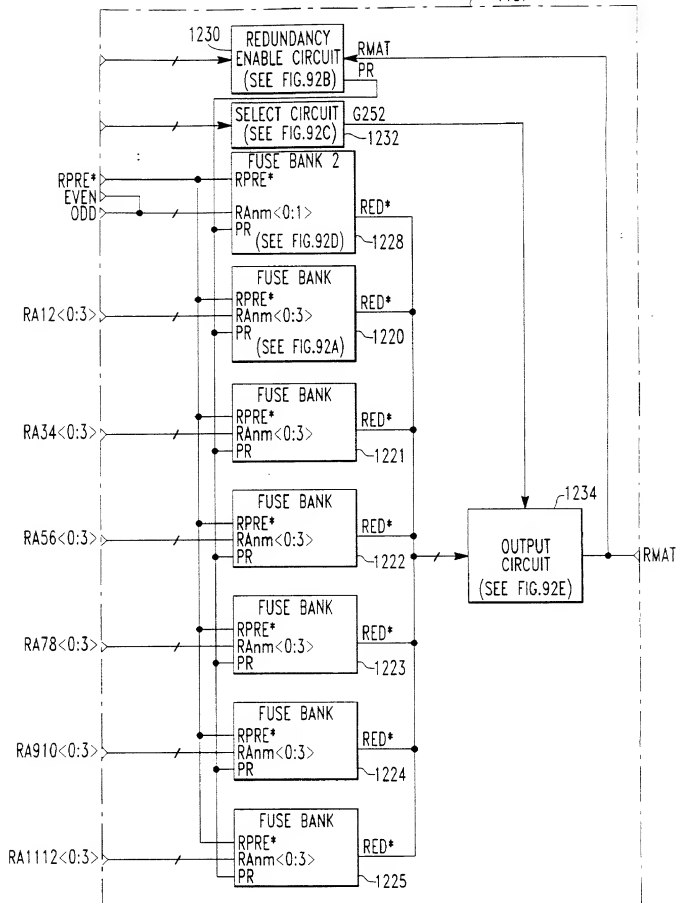


FIG. 91

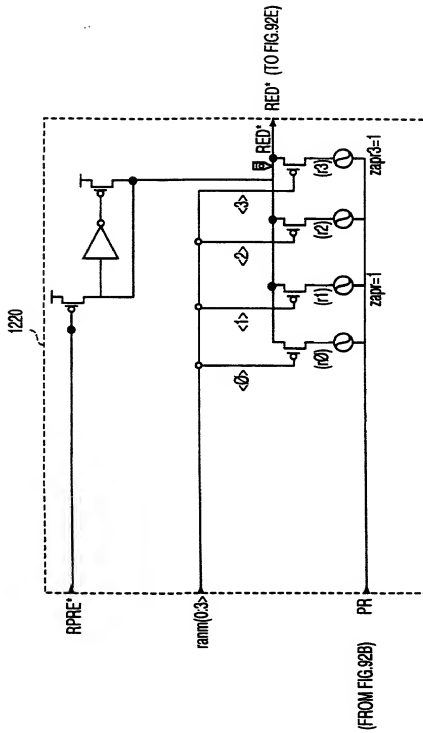


FIG. 92A

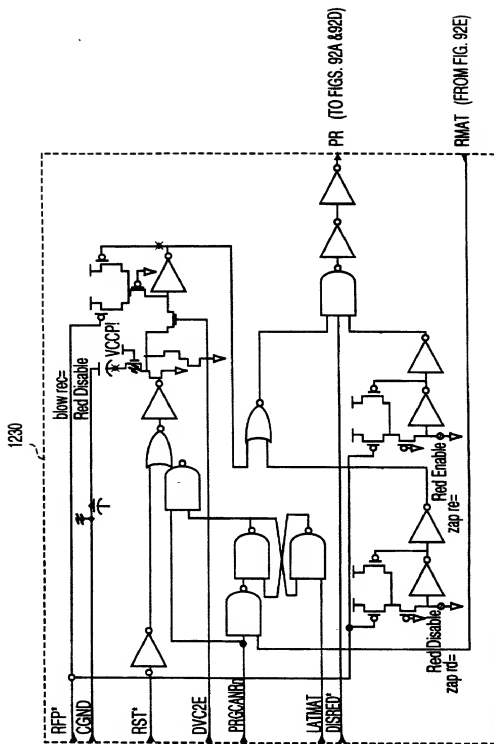


FIG. 92B

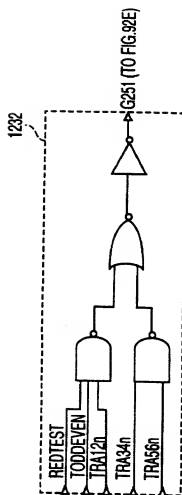


FIG. 92C

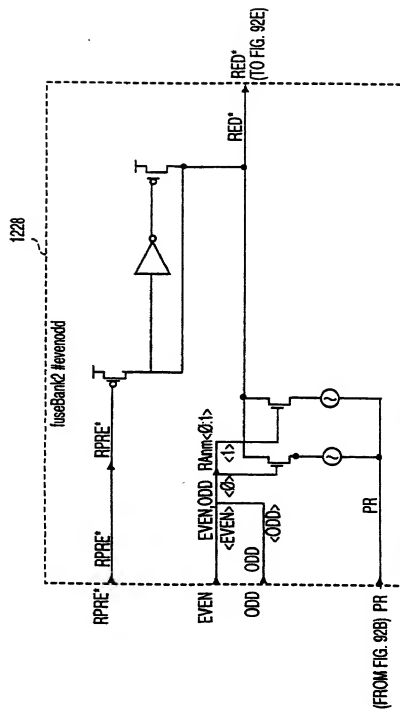


FIG. 92D

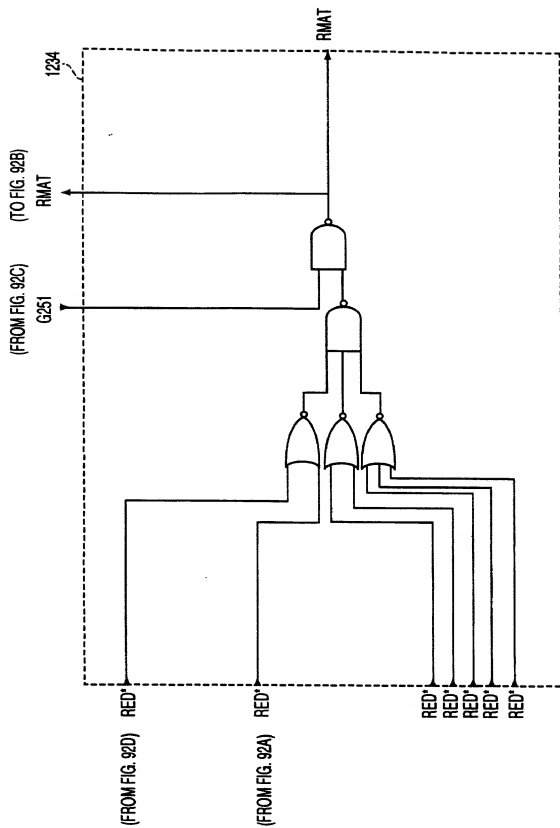
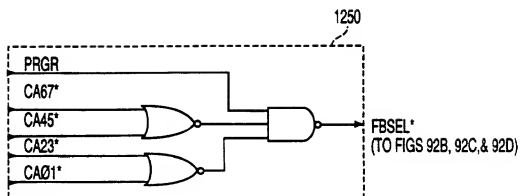


FIG. 92E

**FIG. 93A**

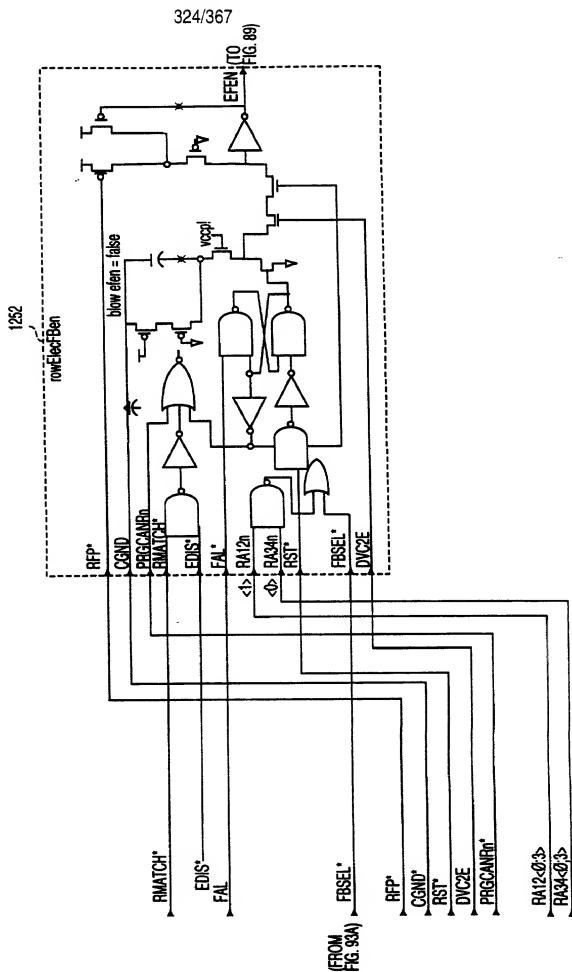
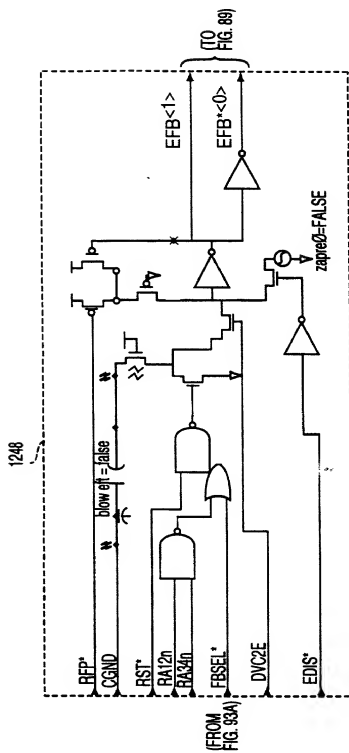
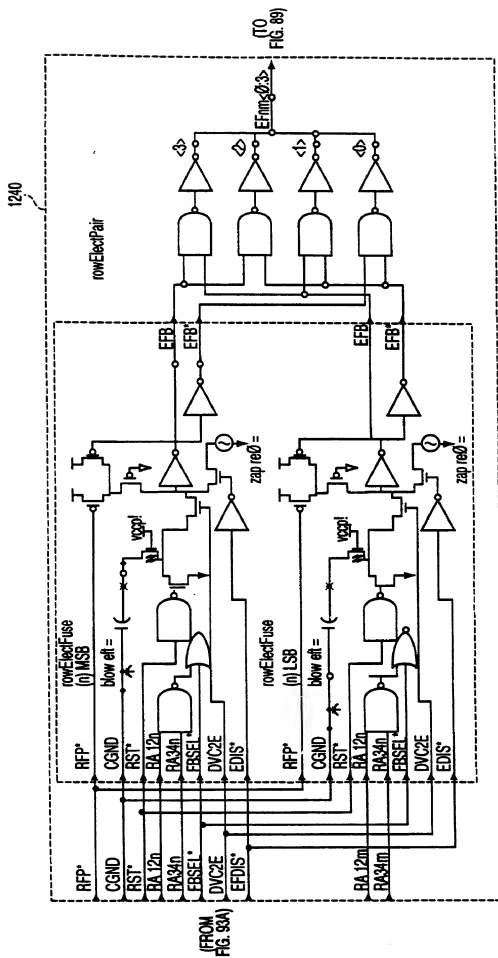


FIG. 93B





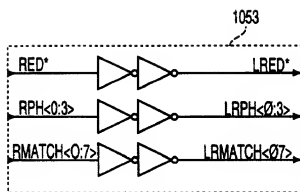
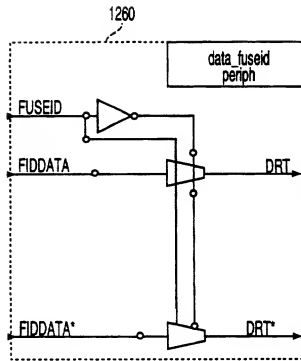
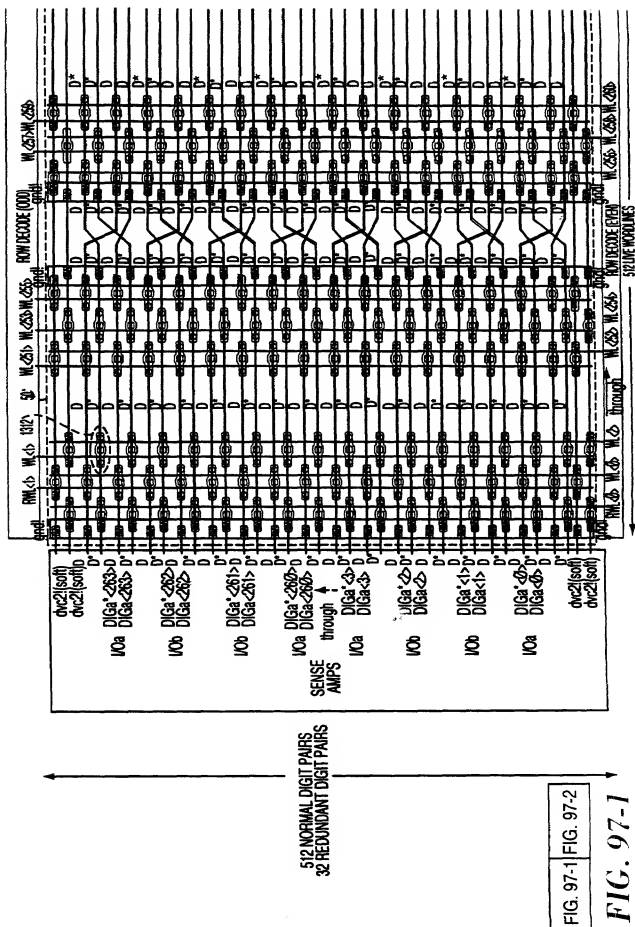
**FIG. 94**



FIG. 95

**FIG. 96**



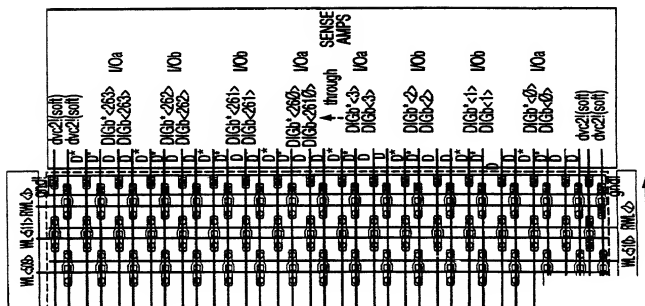
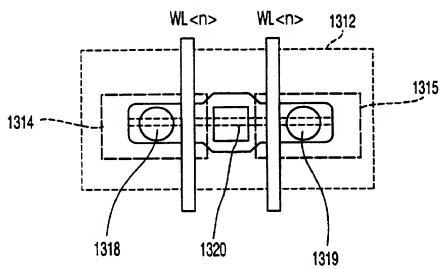


FIG. 97-1 FIG. 97-2

FIG. 97-2

**FIG. 98**

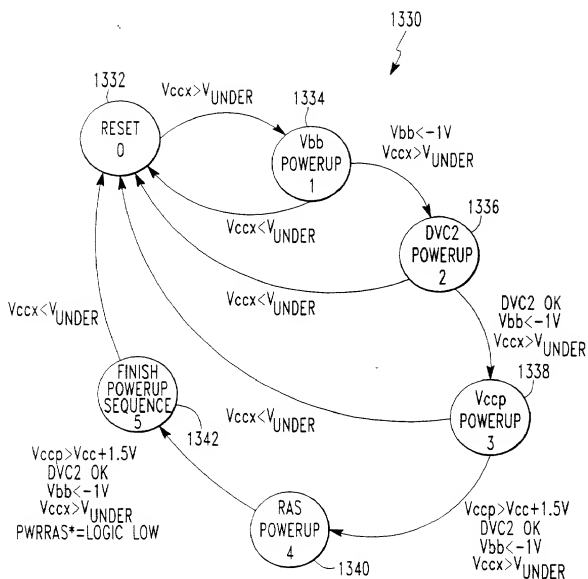


FIG. 99

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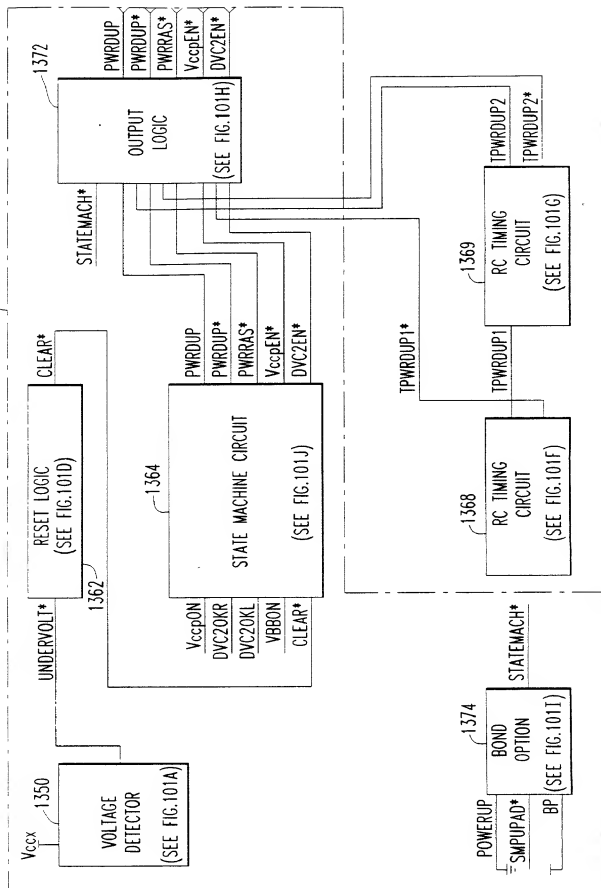


FIG. 100

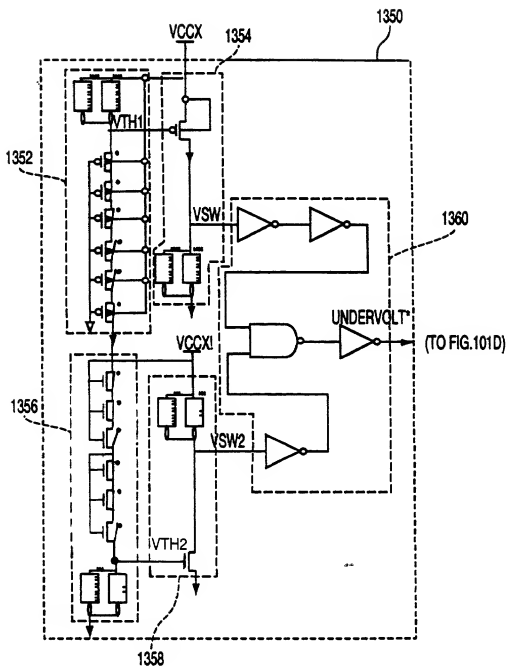
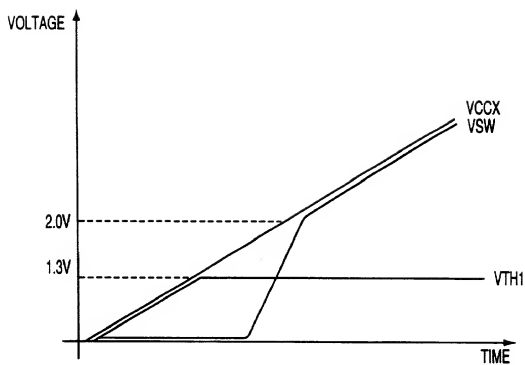
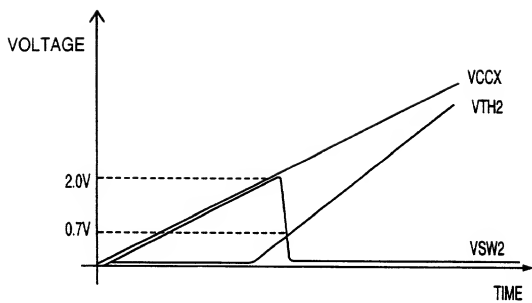


FIG. 101A

**FIG. 101B**

**FIG. 101C**

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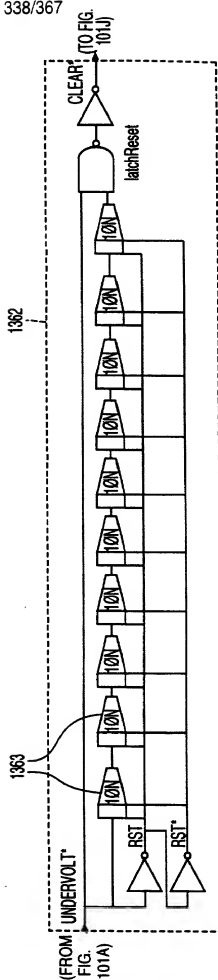


FIG. 101D

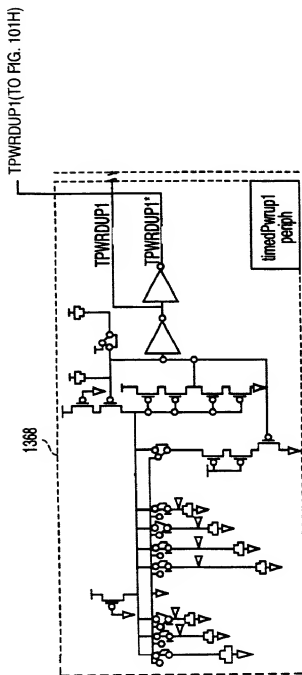


FIG. 101F

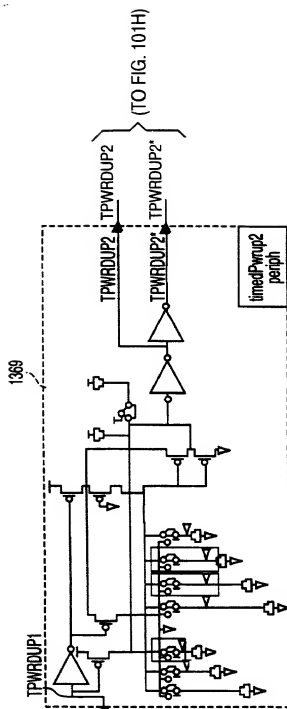


FIG. 101G

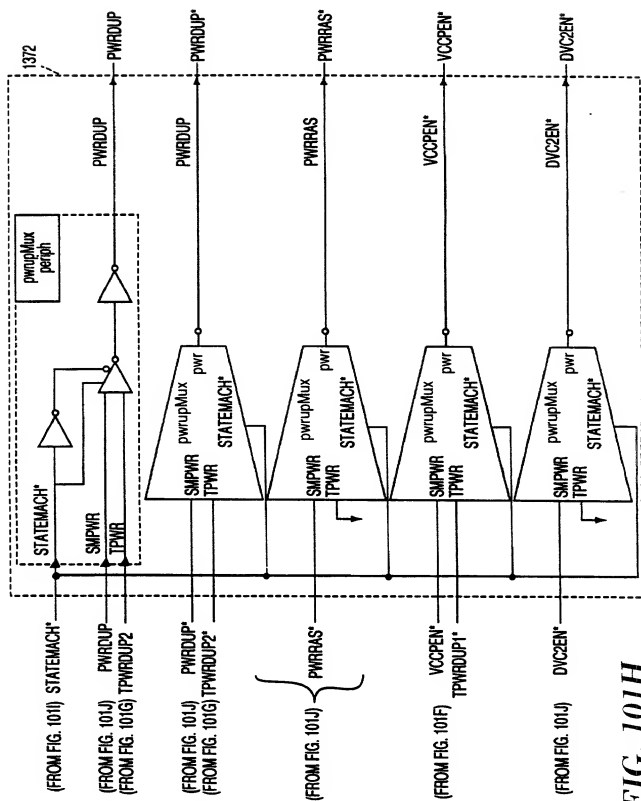


FIG. 101H

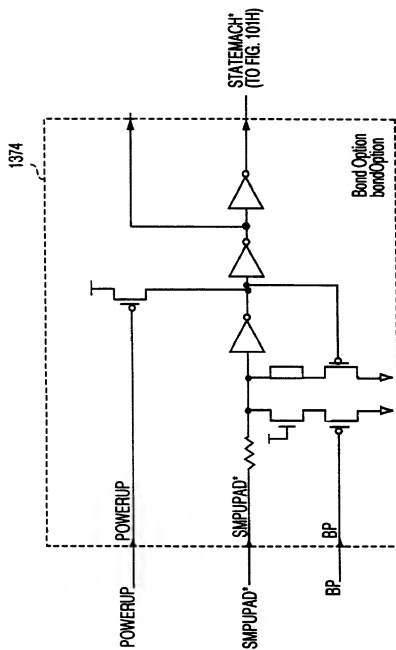
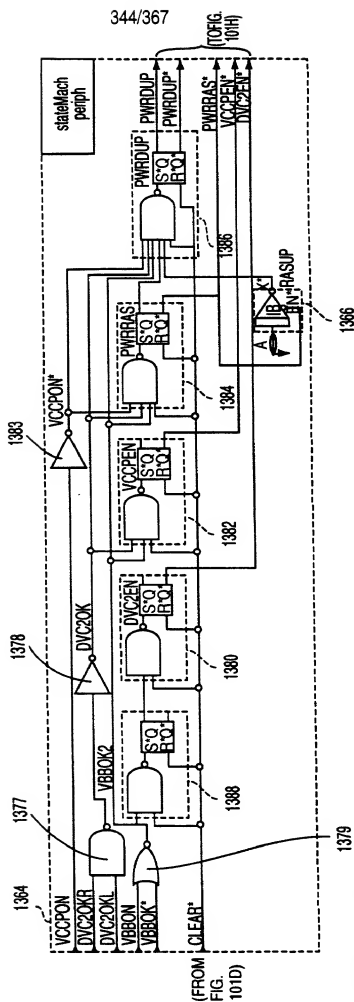
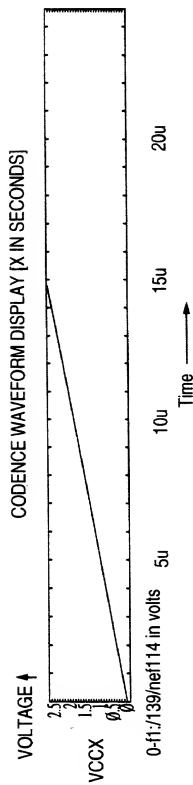


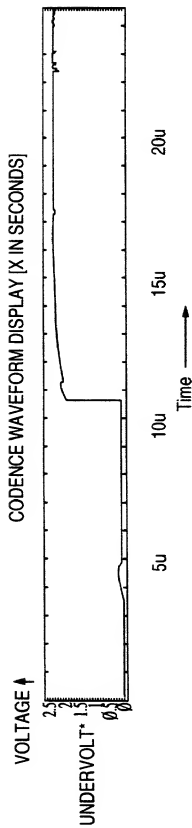
FIG. 1011





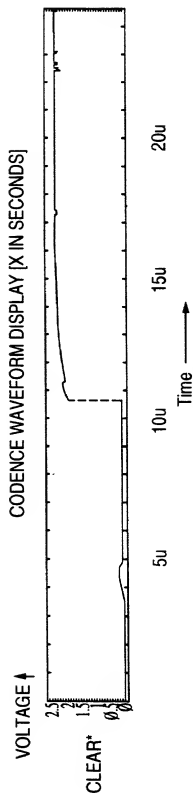
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102A



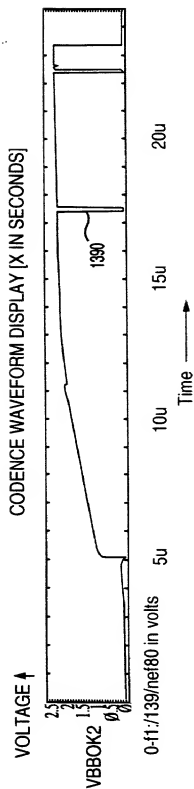
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102B



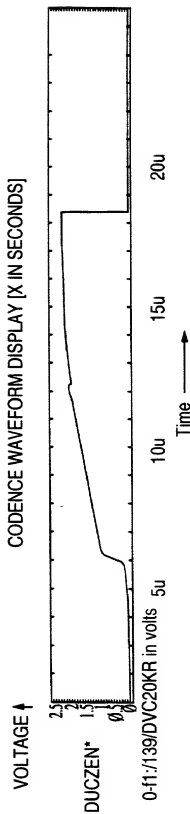
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102C



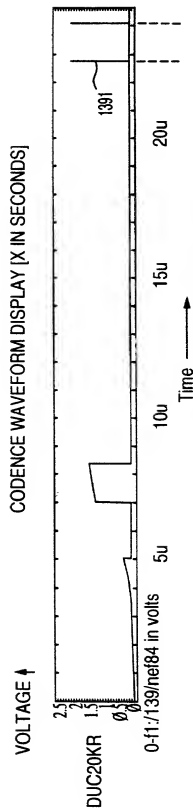
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102D



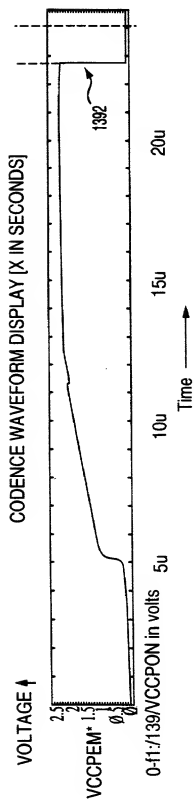
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102E



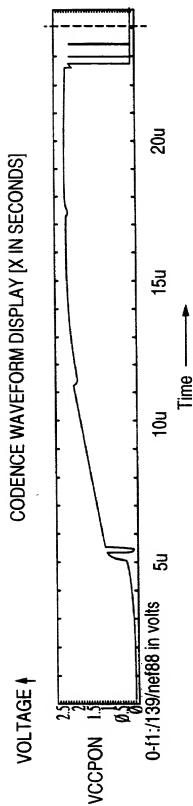
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102F



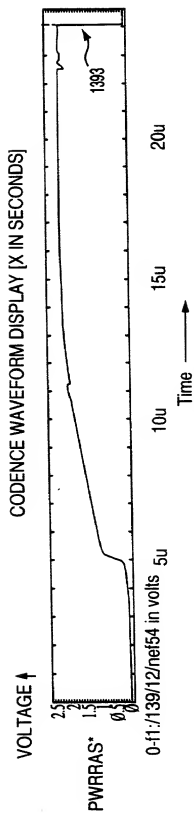
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102C



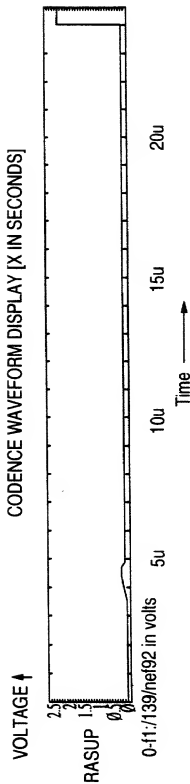
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102H



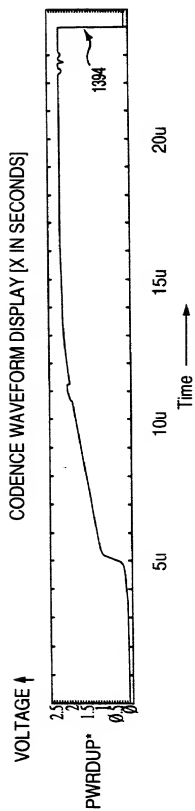
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 1021



NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102J



NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102K

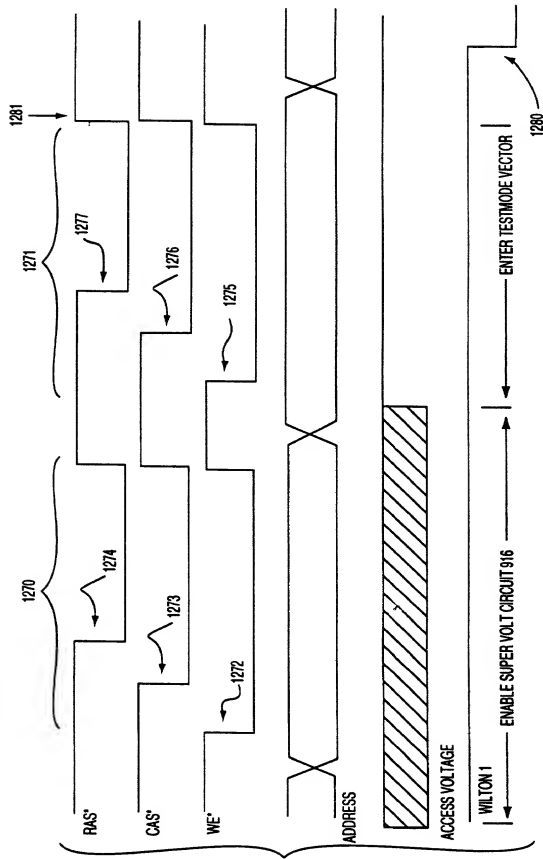
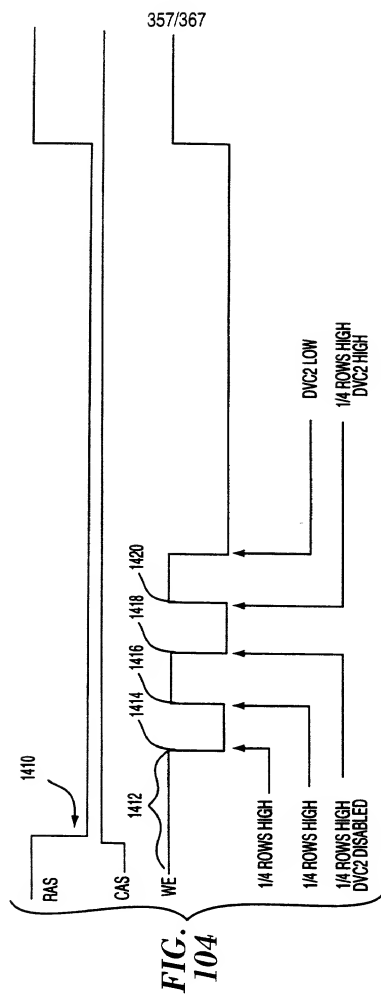


FIG. 103



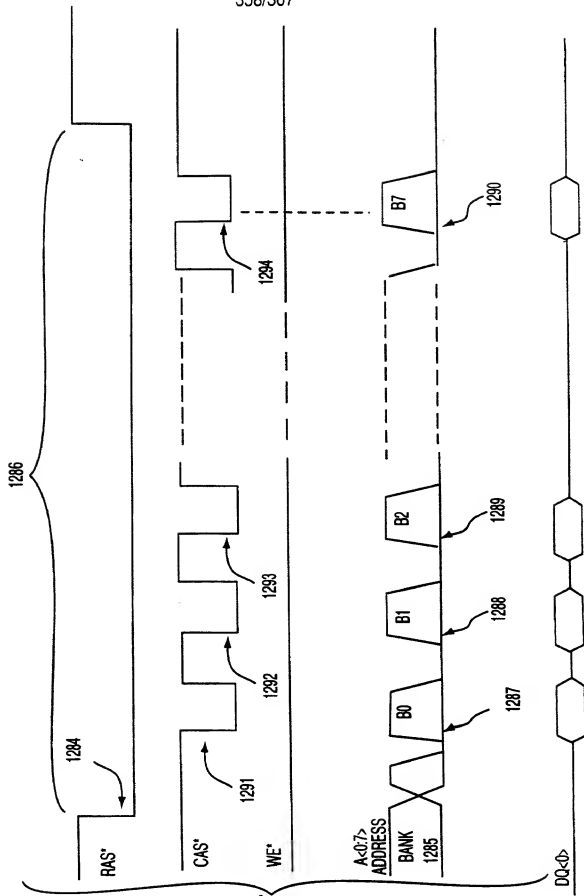


FIG. 105

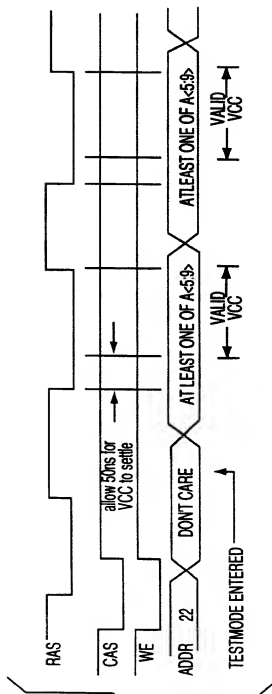


FIG. 106

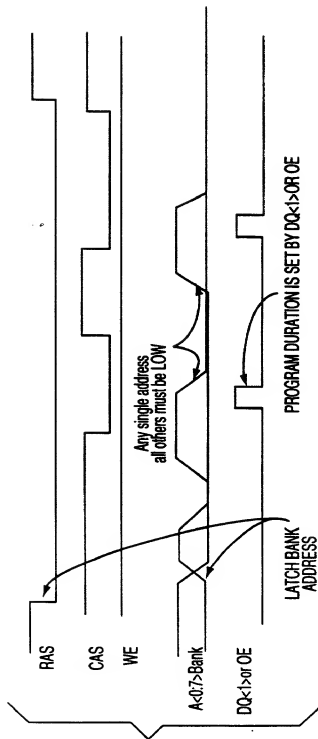


FIG. 107

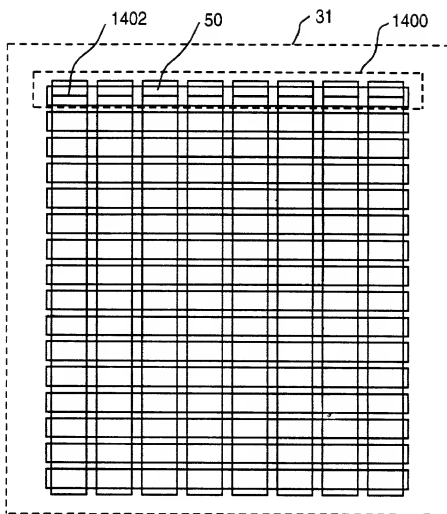
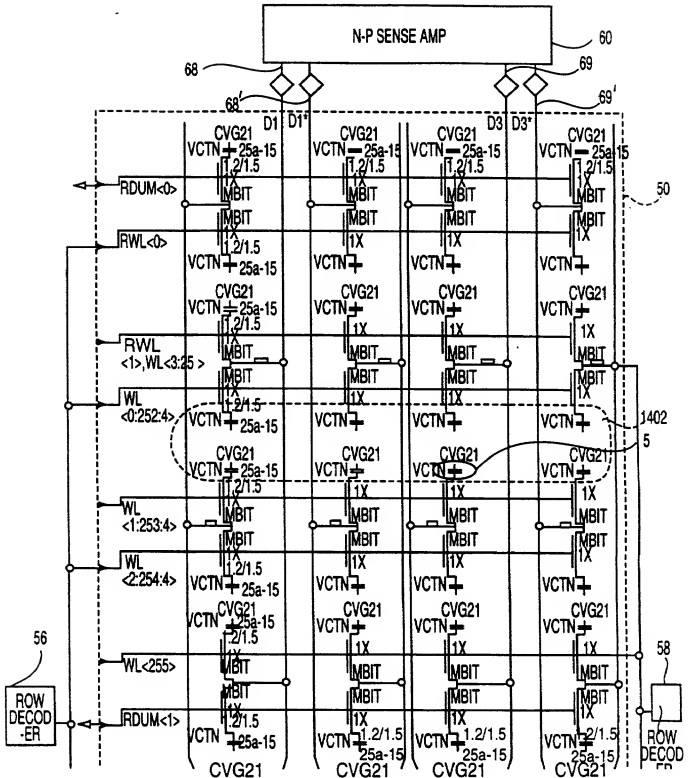
**FIG. 108**

FIG. 109-1

FIG. 109-1

FIG. 109-2



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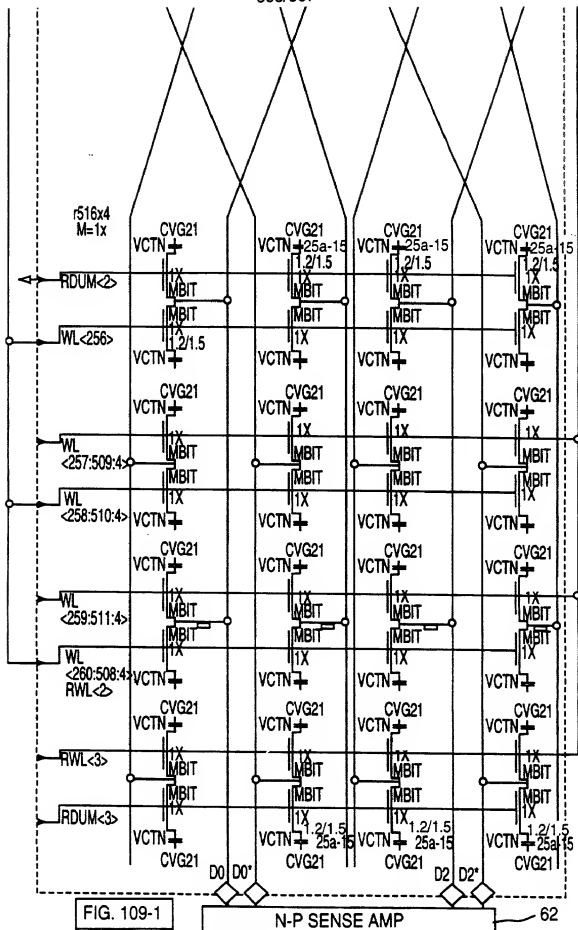


FIG. 109-2

Shrink Factor = 0.24

Mbit = 2.5 x 5.4 μ m (drawn)

0.600 μ m Column Pitch

0.648 μ m Row Pitch

10

63.5 μ m Scribe
24.0 μ m Chg Strip
87.5 μ m Edge

14.999 mm w/scribe
590.53 mils w/scribe

177 μ m

520 total
Wordlines
Wordline
Pitch=
0.648 μ m

Twist
(6.144 μ m)

PN Sense
Arms
(44.66 μ m)

87.5 μ m

87.5 μ m

240 μ m

1024 Actual Digits
Digitline Pitch = 0.500 μ m

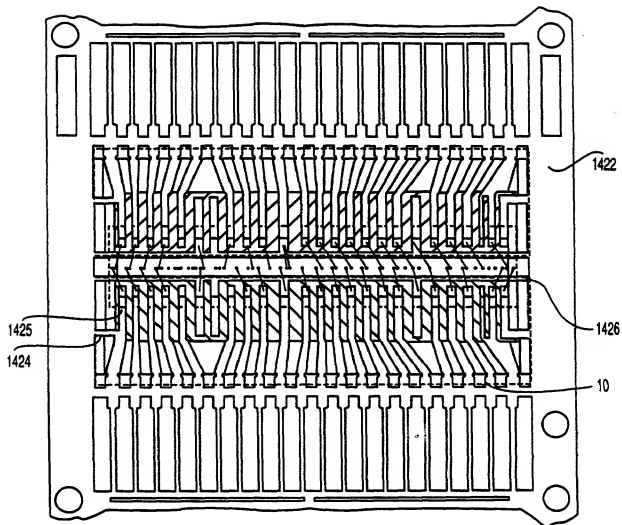
120 μ m

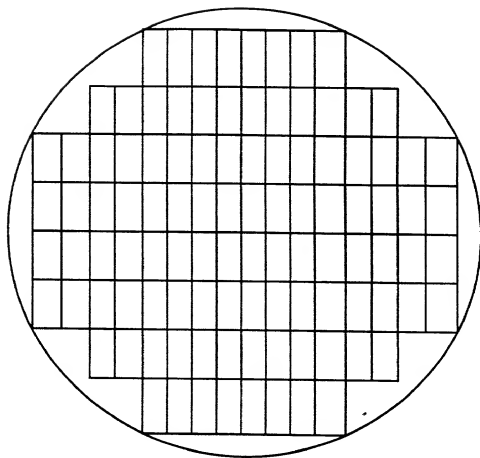
24.677 mm w/scribe
971.55 mils w/scribe

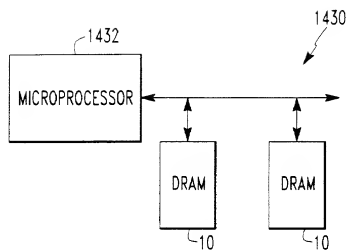
240 μ m

Row Decode (83.12 μ m)
Edge Row Decode (84.72 μ m)
63.5 μ m Scribe
24.0 μ m Chg Strip
87.5 μ m Edge

FIG. 110

**FIG. 111**

**FIG. 112**

*FIG. 113*